Philips DVDR985

Technical Training Manual

Philips Service and Quality/Training
One Philips Drive
Knoxville, TN 37914-1810
P. O. Box 14810
PH: 865-521-4397
FAX: 865-521-4818
EMAIL: TECHNICAL.TRAINING@PHILIPS.COM

PHILIPS

Introduction

This Manual is intended for use by the Service Technician. The first portion of this manual contains a basic description of disc based data playback and recording technologies. Self Diagnostics are included to aid in troubleshooting. Technical Descriptions of the circuitry is followed by a Troubleshooting Section.

The DVDR985 is the forth in a line of DVD recorders. The DVDR1500 was the first. Recordings can be made from broadcast transmissions, and from other analog or digital sources. The DVDRW format allows the user to record and erase a disc many times. The recorded discs will play on most existing and future DVD players. The DVDR985 has a connection for DV or Digital camcorders via an I-Link or Firewire connection. This connection technically is called an IEEE 1394 connection. This machine records on 4.7Gbyte DVD+R and DVD+RW discs. This machine uses a real-time MPEG2 Variable Bit Rate, VBR, Video encoder. The DVDR985 plays back DVD Video, Video CD, Audio CD, CD-R, and CD-RW discs.

Its many features include: Favorite Scene Selection for easy editing, Index Picture Screen for instant overview of contents, Digital Time Base Correcter, Digital Audio output (DTS, AC-3, MPEG, PCM), TruSurround for 3D sound, Zoom + Perfect Still. It is Widescreen, 16:9 compatible, and has a Universal Remote Control, 20 disc resume, Disc Lock, and One Touch Recording.

Virgin Mode

The DVDR985, when first hooked up, needs to get information from the user about what language and what local broadcast system the unit is going to operate with. Use the remote to make those selections. The unit will not operate until this process is completed. If you want the recorder to start up in Virgin mode, unplug the recorder. Plug the recorder in again while holding the STANDBY-ON button.

DVD Basics

Philips with nine other manufacturers chose a format specification for DVDR and RW on March 16, 2001. This new format uses Real Time recording. Its recording is compatible with DVD-Video, and DVD ROM. The data blocks use lossless linking. The physical layout matches very closely that of DVD ROM. See **Figure 1**. It also uses Direct Overwrite when a RW disc is used.

Laser Technology

CDs use a red laser created by a diode and lens system often called a Light Pen. Refer to **Figure 2**. The narrow beam of light is focused onto the reflective layer of a disc. At the instant that focus is achieved, the disc is spun. The laser starts on the innermost tracks of the CD and reads outward. At the beginning of the disc is the Table of Contents. At the bottom of the Light Pen are Monitoring Diodes. The Monitoring Diodes provide information about focus and tracking. Data is retrieved from the disc in the form of pulses of

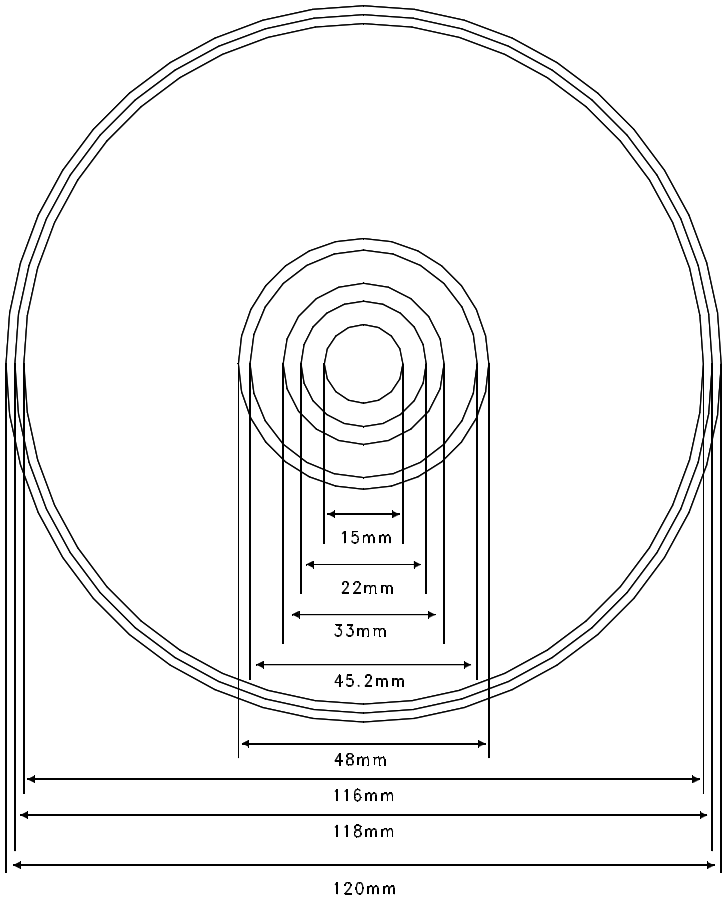


Figure 1 – DVD ROM Disc

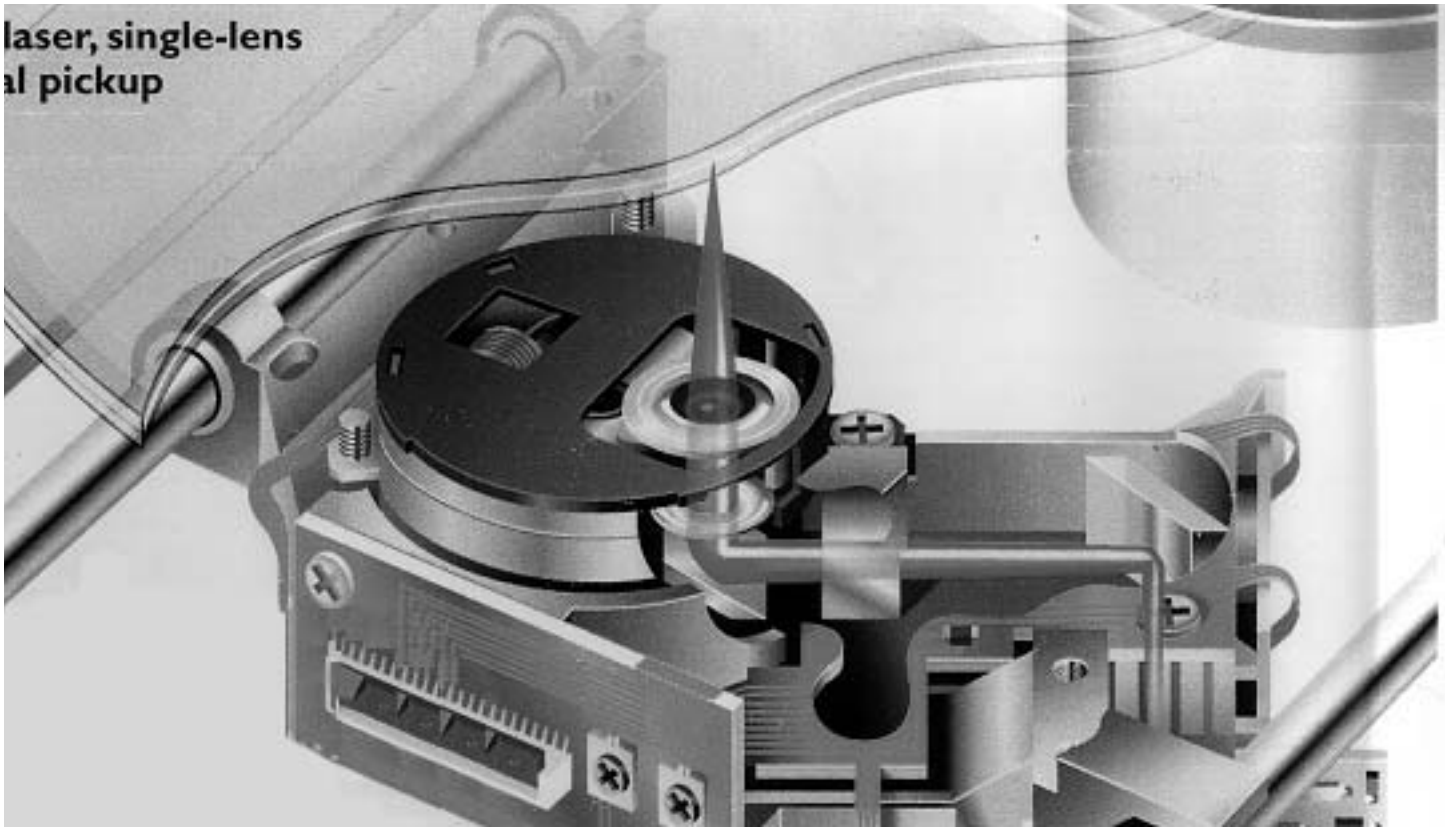


Figure 2 – CD Laser Operation

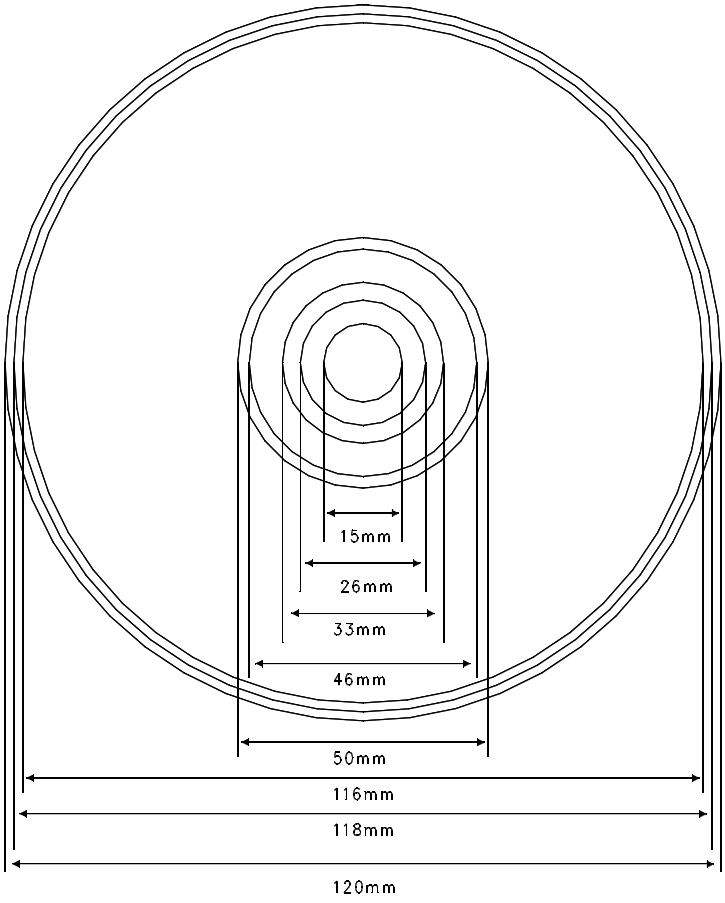


Figure 3 – Mechanical Layout of a CD.

light reflecting from the disc. The pulses are created by Pits in the Reflective Layer of the disc. The Pits reflect less light than the intact surface of the Reflective Layer, called Lands.

Disc Mechanical Layout

The DVD and CD share much of their technology. We will start with CDs and work our way to the DVD. The CD is a plastic disc 120mm in diameter, with a thickness of 1.2mm. **Refer to Figure 3**. It has a silver colored Reflective Layer. The maximum playing time for a music recording on a Compact Disc, CD, is 74 Min.

The CD is less vulnerable to damage than an analog record. That does not mean it does not have to be treated with care. Dirt and heavy scratches can interfere with playability.

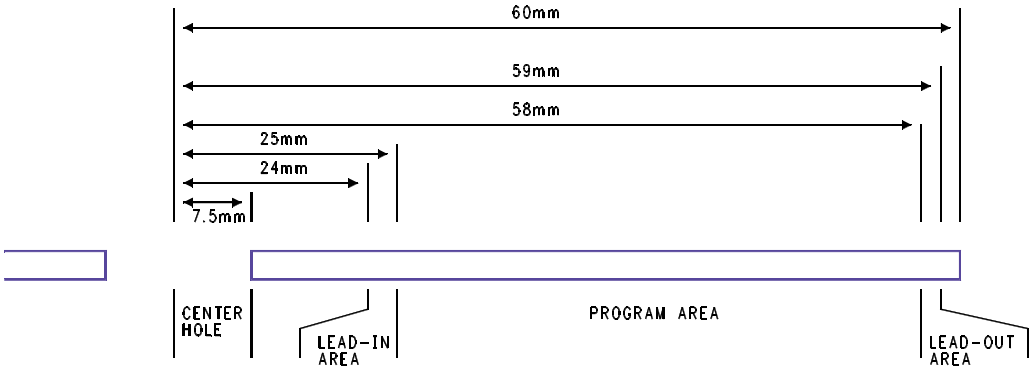


Figure 4 - The Disc

As shown in **Figure 4**, the CD is subdivided into three parts: the Lead In Track, the Program Area, and the Lead Out Area. These three sections together are considered the Information Area. There is a hole in the center for holding the disc. The disc is held between two equally sized concentric rings. The rings have an inner diameter of 29mm and an outer diameter of 31mm.

The Data on the disc is recorded on a spiral shaped track with pits and lands. The reflective side of the disc contains the tracks.

The production of a disc is a high tech process explained in **Figure 5**. The process starts with glass that is photo etched. The glass is silver plated and is used as a form for a metal cast. The metal cast is used to stamp a nickel Mother Stencil. The Mother Stencil is used to stamp the Son Stencil. Son Stencils are used to stamp the foil of the discs. A protective layer and label are added.

Read Process

The Servo circuit is responsible for focusing the laser and moving the Light Pen to follow the spiraling tracks on the rotating disc. The digital High

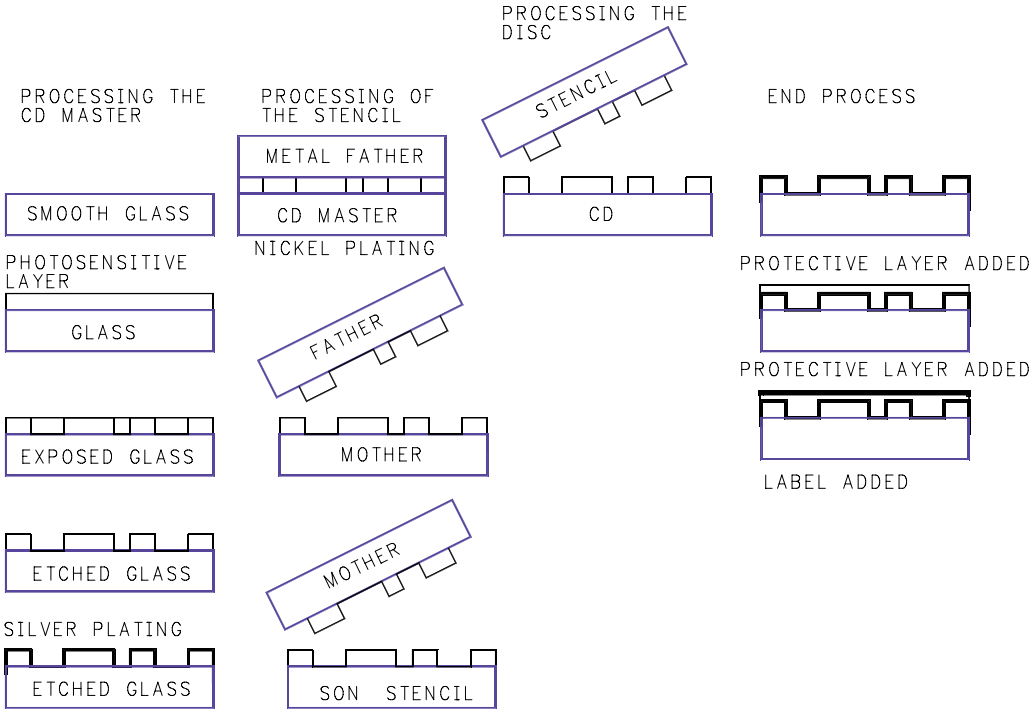


Figure 5 - Creating a CD

Frequency information, HF, is demodulated and stored in RAM. When the RAM is half full, the data is fed out to the Digital to Analog Converters. The speed of the rotating disc is servo controlled to keep the RAM half full. The analog signals are amplified and sent to the output connectors.

A partially recorded disc's Information Area has four sections: a PCA/RMA area, a Lead In Area, a Recorded Program Area, and a Recordable Program Area. See **Figure 6** for the dimensions. The PCA Area is the Power Calibration Area, PCA. The RMA Area is the Recording Management Area.

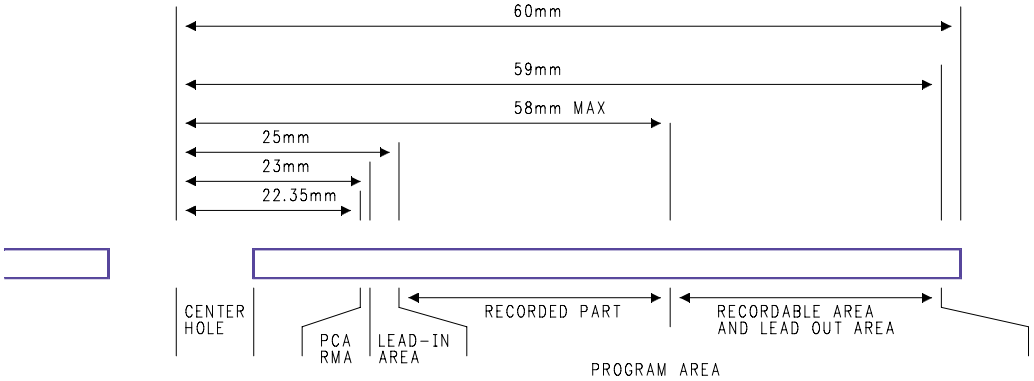


Figure 6 – A Partially Recorded Disc.

Record Once Technology

Disc Mechanical Layout

From an external point of view, a DVD is the same as the CD. Recordable media creates the need for three physical layouts. There are three possible states of a disc: a blank disc, a partially recorded disc, and a full or finalized disc. The difference is in the way the Information Area is divided. The Information Area of a blank disc extends from 22.35 mm centered on the disc to 59 mm centered on the disc. Refer to **Figure 6.**

A fully recorded or finalized disc's Information Area has three sections: A lead in Area, the Program Area, and the Lead Out Area. See **Figure 7** for the dimensions.

The disc's recordable layer contains major differences from that of a stamped disc. The blank disc has a Pre-groove stamped into the recordable layer of the disc. This is polycarbonant for DVD+Rs and organic dye material for DVD+RWs. This spiral Pre-groove is for the Servo circuit to provide a mechanical reference

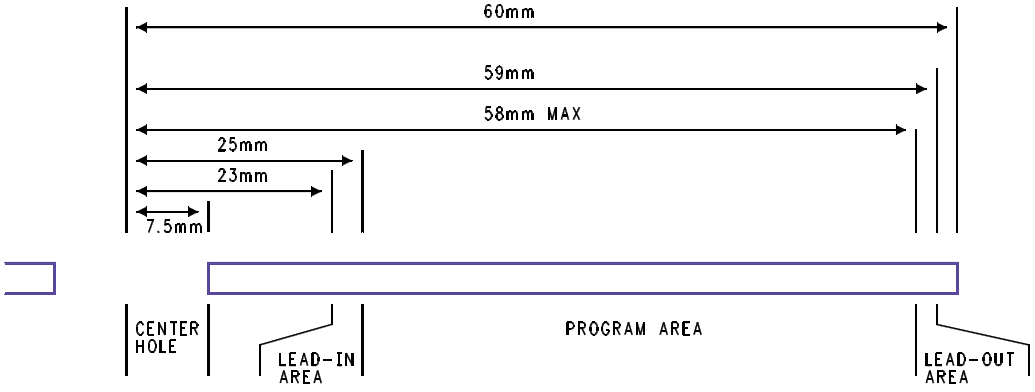


Figure 7 – Fully Recorded or Finalized Disc

during recording. The dye based RW recordable layer provides a reflectivity of 40% light return and 70% light return. 40 percent reflectivity represents Pits and the 70% represent the Lands.

Record Process
The record process shares most of its mechanical operation with that of the play process. The main difference is how the Servo is locked to the disc. The Servo follows the Pre-groove for Radial Tracking and disc speed. The speed of the disc is locked to a wobble signal that is part of the spiral grove stamped into the disc.

The intensity of the laser beam is modulated from playback intensity to write intensity. As the disc reads the Pre-groove, the laser arrives at a position where a Pit is to be formed. The laser power increases from 4mW to 11mW. This raises the temperature of the disc to 250 degrees Celsius. The recordable layer melts, reducing its volume. The polycarbonate flows into the space vacated by the dye. The modulation from read laser power to write laser power forms a pit and land pattern effectively the same as a prerecorded disc.

Re-recordable Technology

Disc Mechanical Layout
Disc usage mechanically is identical to the recordable media. The only difference is the chemical make up of the recordable layer. The recordable layer is made up of an alloy of silver, indium, antimony and tellurium.

Re-Recording Process
The Re-Record process shares much of its operation with that of a CDR. The blank disc's Information Area is in a polycrystalline state. During recording, the laser power is modulated from 8mW to 14mW. 8mW is the playback laser power and 14mW is the record laser power. The polycrystalline state of the recordable surface changes, or melts at 500-700 degrees C into an amorphous state. The melted, amorphous areas reflect light less than the crystalline areas, creating a pattern similar to the stamped CD. A major difference of CDRWs from CDRs is the ability to erase.

The Erase Process
To Erase a CDRW disc, the recordable layer must be returned to its polycrystalline state. This is done by heating up the temperature of the recorded surface to 200 degrees C. This is less than the melting point. This is done at X2 recording speed. The slower speed allows time for the alloy to return to its proper state. This takes approximately 37 min. Some software erases the just the TOC on the disc and allows the disc to be rewritten. This method is not as reliable

Over Writing Process
Overwriting combines the processes of erasing and writing. When the disc and Light Pen are in position to start writing the new data, the laser power starts modulating in the same manner as it does for normal recording with one difference. During the time there is to be a land, the laser power goes to the erase level rather than the playback level.

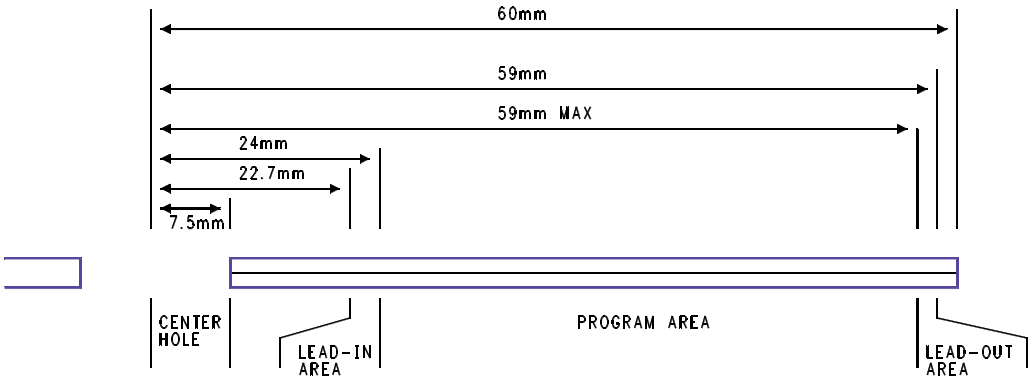


Figure 8 – Mechanical Layout of a DVD

DVDs

All of the previously discussed technologies apply to the DVD. Like CDs, DVDs are also stamped into play only discs. In this discussion, we will point out the differences between DVDs and CDs. If you are new to disc based technology, you will want to start with the information preceding this discussion.

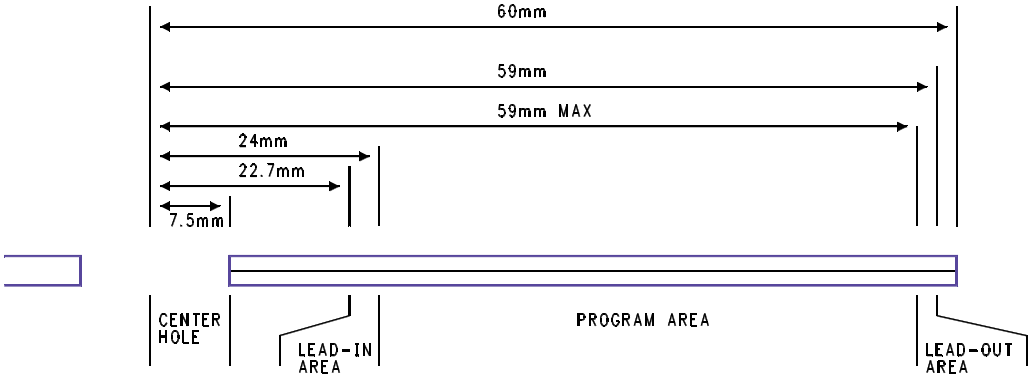


Figure 8 - DVD Mechanical Layout

DVD Disc Mechanical Differences

Most DVDs are single sided, however, the DVD specification allows for two readable layers, and the disc can be double sided. We will start our discussion with single sided, single layered discs. A Digital Versatile Disc, DVD, looks very similar to a CD. Refer to **Figure 8**. The Clamping Area is larger, starting at 11 mm centered to 16.5 mm centered. The Lead In Area is smaller, measuring 22.7 mm centered to 24 mm centered. The Information Area is limited to 116mm centered.

Two of the big differences between DVDs and CDs are the Pit and Land sizes, and the track widths. Refer to **Figure 9.**

The Manufacturing process of a DVD is comparable to that of a CD. The main difference is the thickness. The DVD can be a double sided product. Each side is .6mm. The two sides are glued back to back, producing 1.2mm total thickness.

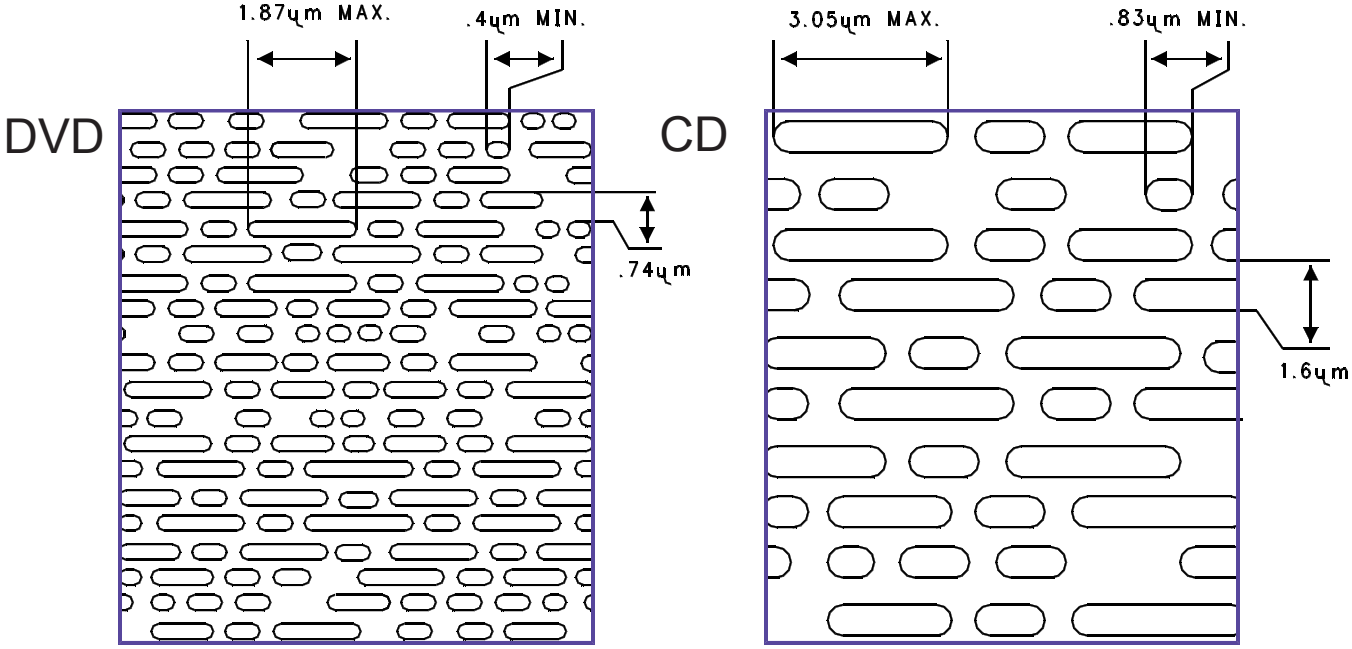


Figure 9 – DVD and CD Pit Structure.

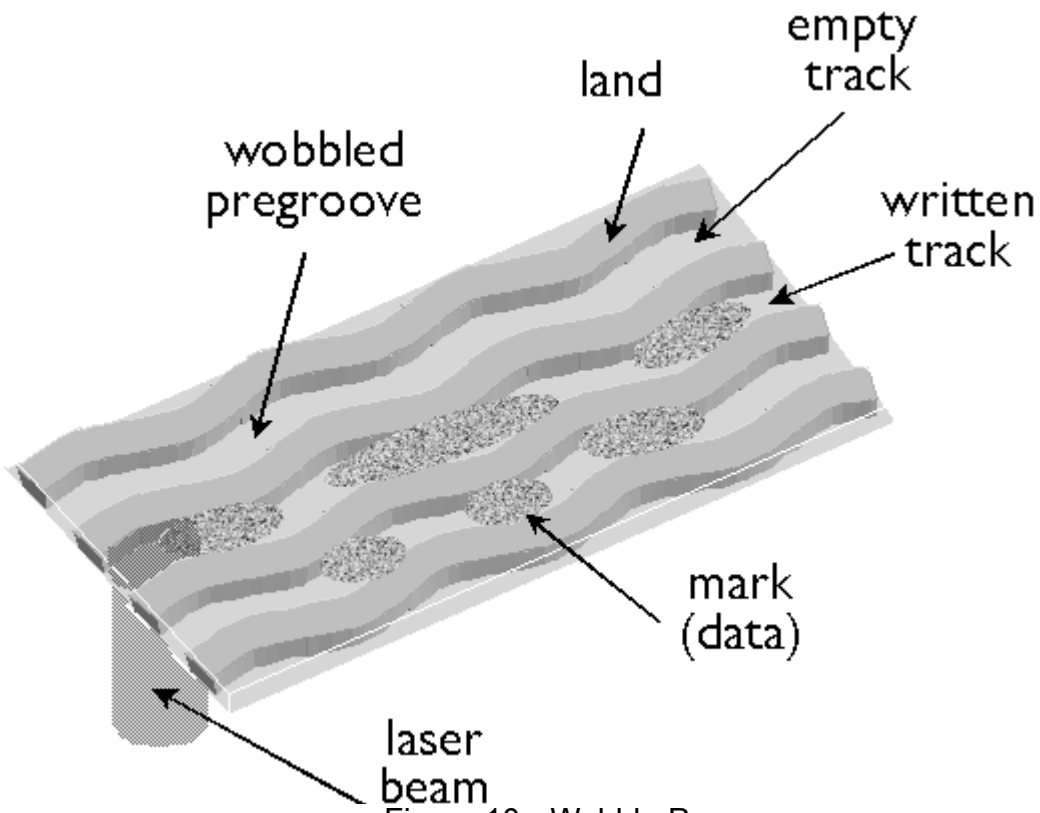


Figure 10 - Wobble Pregroove

Wobble

A Pre-groove is stamped on writable discs. All recordable DVD media types feature a microscopic wobble groove embedded in the plastic substrate. This wobble provides the recorder with the timing information needed to place the data accurately on the disc. During recording, the drive's laser follows this groove, to ensure consistent spacing of data in a spiral track. The walls of the groove are modulated in a consistent sinusoidal pattern, so that a drive can read and compare it to an oscillator for precise rotation of the disc. This modulated pattern is called a wobble groove, because the walls of the groove appear to wobble from side to side. This signal is only used during recording, and therefore has no effect on the playback process. Among the DVD family of formats, only recordable media use wobble grooves.

Dual Layer Discs

Two information layers are separated by a thin transparent layer. Refer to **Figure 11**. The first layer is partially transparent. This allows the second layer to be read through the first layer. Both layers are read by controlling the focus. There are two methods for reading the data of a Dual Layer disc, PTP and OTP. Refer to **Figure 12**.

PTP is Parallel Track Path. That means the Lead In and Out Areas of the two layers correspond to each other. Each Lead In Area is on the inner portion of the disc, and the Lead Out Area is on the outer portion of the disc. This is useful to link data between the layers.

Figure 11 – Dual Layer DVD

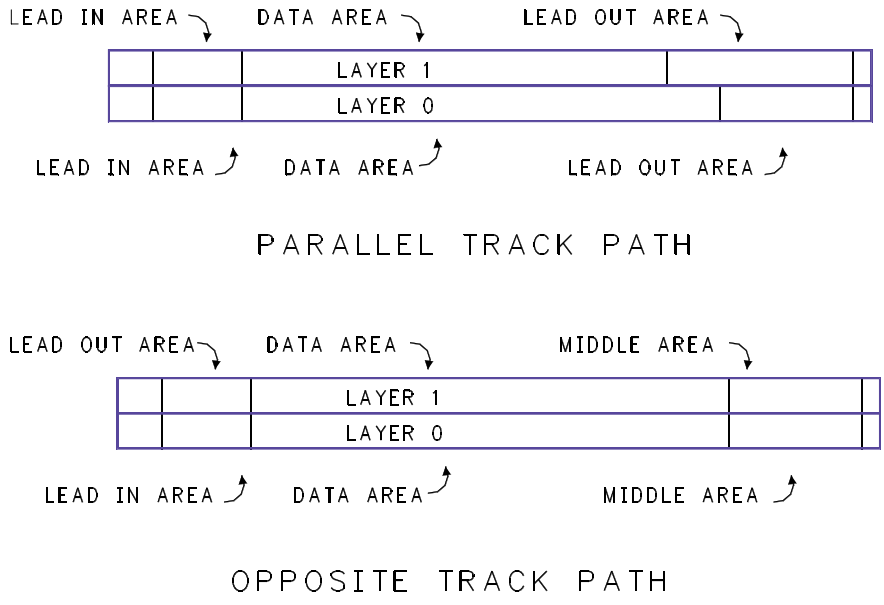


Figure 12 – PTP and OTP Layout

This allows instant access to the additional data or scene. OTP is Opposite Track Path. This method links the end of one layer to the beginning of the other. The Lead In Area is still on the inner portion of the disc. There is a Middle Track Area on both of the layers located on the outer portion of the layers. The Middle Track Area links the data on the two layers together. The Lead Out Area is on the second layer on the inner portion of the disc.

Capacity

Because a stamped DVD can be Dual Layered and Double Sided, there are four different capacities. Refer to **Figure 13**. These capacities strictly pertain to raw data. The time available for Video and Audio has many extra factors that determine the length of time on each side or layer. The picture complexity and the amount of movement in the picture affect compression and time on a disc. The number of languages affect the time on a disc. The type and quality of the Audio has an affect on the time also. It can be mono, stereo, or AC-3. Therefore, the media itself determines the capacity in time on the disc.

DISC SIZE	DVD	CD	TYPE
8cm	1.4Gb	1.9Mb	SL/SS
	2.6Gb	X	DL/SS
	2.9Gb	X	SL/DS
	5.3Gb	X	DL/DS
12cm	4.7Gb	680Mb	SL/SS
	8.5Gb	X	DL/SS
	9.4Gb	X	SL/DS
	17Gb	X	DL/DS

Figure 13 – DVD Multi-Layered Capacities

Automatic Self Diagnostic Modes
(End User/Dealer Script Interface)

Description

The End User/Dealer Self Diagnostics work without the need for other equipment. A number of hardware tests are automatically executed to check for faults in the recorder. The diagnosis ends with a “FAIL” or “PASS” message. If the message “FAIL” appears on the display, an Error Code is displayed. If the message “PASS” appears, the tests have been executed successfully. There can still be a failure in the recorder. The tests do not cover the complete unit. The following list describes the tests being preformed while the test number is being displayed on the Front Panel. To place the unit in the Self Test Mode, hold the Play pushbutton on the Front Panel while suppling AC power to the unit. The display counts down numerically the test it is performing.

The following is a list of the test displayed as:

“Test Number” is displayed on the Front Panel
“Name”of the test
Description of the test

22
SdramWrR
Checks all memory locations of the 4Mbyte SDRAM

21
HostdDramWrR
Checks all the DRAM connected to the microcomputer on the Digital Board

20
HostdI2cNvram
Checks the data line (SDA) and the clock line (SCL) of the I2C bus between the host decoder and NVRAM

19
SAA7118I2c
Checks the interface between the Host I2C controller and the SAA7118 Video Input Processor

18
VideoEncI2c
Checks the interface between the host I2C controller and Empress

17
AudioEncI2c
Checks the I2C connection between the host decoder and Empress

16
AudioEncAccess
Tests the HIO8 interface lines between the host decoder and the audio encoder

15
AudioEncSramAccess
Checks the access of the SRAM by the audio encoder (address and data lines).

14
AudioEncSramWrR
Tests the SRAM connected to the audio encoder

13
AudioEncInterrupt
Tests the interrupt line between the host decoder and the audio encoder

12
VsmAccess
Checks whether the VSM interrupt controllers and DRAM are accessible

11
VsmInterrupt
Checks both interrupt lines between the VSM and the host decoder

10
VsmSdramWrR
Tests the entire SDRAM of the VSM

9
Clock11.289MHz
Switches the A_CLK of the micro clock to 11.2896 MHz

8
Clock12.288MHz
Switches the A_CLK of the micro clock to 12.288 MHz

7
BeS2Bengine
Checks the S2B interface with the Basic Engine by sending an echo command

6
DisplayEcho
Checks the interface between the host processor and the slave processor on the display board

5
AnalogEcho
Checks the interface between the host processor and the microprocessor on the Analog Board

4
AnalogNvram
Checks the NVRAM on the Analog Board

3
Tuner
Checks whether the Tuner on the Analog Board is accessible

2
LoopAudioUserDealer
Tests the components in the audio signal path: The host decoder on the Analog Board, the audio encoder, the VSM. The Audio is internally looped back thru the Digital Board

1
LoopVideoUserDealer
Tests the components on the Video signal system path: - The VIP- The Video encoder- The VSM- The host decoder. The Analog Board On Video signal is internally routed back to the Digital Board.

Color bars appears on the output. It is a PAL colorbar pattern which means you may see a greyscale bar pattern. The pull in range of the monitor, will affect what is seen. An NTSC color bar signal can be output from the Host Decoder using ComPair.

Manual Service Diagnostics
(Player Script)

Description

The Manual Diagnostics provide the opportunity to perform tests and exercise the unit in a way that helps determine which of the DVD recorder's circuit boards are faulty. If no Errors are found, it performs an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set. The Servicer must respond to what is seen and heard on the monitor. (i.e. to approve a test picture or a test sound). Some tests require that a DVD+RW disc be inserted.

Structure of the Player Script
The player script (Manual Diagnostics) tests the circuit boards in the DVD recorder: the Display PCB, the Digital PCB, the Analog In/Out PCB and the Basic Engine.

The Player tests are done in two phases, interactive tests and a burn in test. The interactive tests depend strongly on user interaction and input to determine the results and to progress through the full test. The Burn-in Loop test will perform the same set of tests as the dealer test, but it will loop through the list indefinitely. Is is especially usful if you reset the Error Log. You can do this using ComPair. You can then read the error codes using ComPair.

Step by Step Description

1
Press **OPEN/CLOSE** and **PLAY** buttons at the same time and provide AC to the recorder to start the player script. Press **Play** to perform the test described on the display. Press **Stop** to skip the test and go to the next test. Press **Record** to indicate to the Microcomputer the desired result malfunctioned.

2
The display shows **FP SEGM**. Press PLAY to start the test. First the starburst pattern is lit, then the horizontal segments are lit, followed by the vertical segments and the last test lights all the segments. After each of the four tests, the user has to confirm that the correct pattern was lit. Press PLAY to confirm that the correct pattern was lit (four times if the FPSEGMENTS test was successful). Press **RECORD** to indicate that the correct pattern was not successfully lit. Press **STOP** to skip this test.

3
The display shows **FPLABELS**. All labels should be lit

4
The display shows **FPLIGHT ALL.** Everything should be lit.

5
The display shows **FPLED**. The LED changes color.

6
The display shows **FP LED**. The red Record light comes on. Press play to confirm it lit.Press STOP to skip this test.

7
The display shows **FPKEYBRD**. All keys have to be pressed to get a positive result! This includes the Power button. Press PLAY for more than two seconds to confirm that all the keys were pressed and that it was shown on the display. Press STOP for more than one second to skip this test.

8
The display shows **FP REMCTL.** Press PLAY to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result.

9
The display shows **FPDIMMER**. Press PLAY to activate the dimming feature. Press Play to confirm that the text on the local display was dimmed.

10
The display shows **ROUTE VID**. Press Play to advance.

11
The display shows **ROUTE AUD**. Press Play to advance.

12
The display shows **COLORBAR ON**.Press Play to advance. An NTSC Colorbar Pattern should apear at the output. Press play to advance.

13
The display shows **PINKNOISE ON**. The monitor should produce Pink noise.

14
The display shows **PINKNOISE OFF**. Press Play to advance.

15
The display shows **BE RESET**. Press PLAY to Reset the Basic Engine (Mechanism/Servo PCB).

16
The display shows **BE TRAY OPEN**. Press PLAY to open the tray. Place a RW disc in the tray.

17
The display shows **BE TRAY CLOS**. Press PLAY to close the tray.

18
The display shows **BE WRITE READ**. This requires a RW disc to be in the machine. The BE resets and a small write is preformed, and then a read. this will take 20 seconds or so.

19
The display shows **BE TRAY OPEN**. This opens the tray.

20
The display shows **BE TRAY CLOS**. This closes the tray.

21
The display shows **ERRORLOG READ**. If there was an error a code will be displayed. If you press PLAY, the User/Dealer script will start an endless loop. If the unit fails a test, the local display will display FAIL and the error code

In case of failure, the display shows " **FAIL XXXXXX** "The description of the shown error code should be found in the list to follow. Once an error occurs, press the STOP key to jump over the failure and to continue the diagnostics.

There is a Error Code Table in Force Manual 2064

10000 - Checksum is OK

10001 -Segment name Checksum doesn't match or segment name segment not found

10101 - FLASH 1 Write access test failed

10201 - FLASH 2 Write access test failed

10301 - FLASH write test failed

10302 - FLASH write command failed

10303 - FLASH write test done max. number of times

10401 - HostDec SDRAM Memory data bus test fails.

10402 - HostDec SDRAM Memory address bus test fails.

10403 - HostDec SDRAM Physical memory device test fails.

10501 - HostDec SDRAM Memory data bus test fails.

10502
HostDec SDRAM Memory address bus test

fails.

10503
HostDec SDRAM Physical memory device test fails.

10601 - HostDec DRAM Memory data bus test fails.

10602 - HostDec DRAM Memory address bus test fails.

10603 - HostDec DRAM Physical memory device test fails.

10701 - HostDec DRAM Memory data bus test fails.

10702 - HostDec DRAM Memory address bus test fails.

10703 - HostDec DRAM Physical memory device test fails.

10800 - Host Decoder version (cut) number: version number Digital hardware version

10801 - Can not find version in FLASH.

10901 - Error muting Audio

11001 - Error un-muting

11501 - Init of I2C failed

11502 - The selection of the clock source failed

11504 - The un-mute of the Audio failed

11601 - Init of I2C failed

11602 - The mute of the Audio failed

11701 - Init of I2C failed

11702 - The muting of the Audio failed

11703 - The un-mute of the Audio failed

11704 - The selection of the clock source failed

11707 - Setup of Front panel failed

11708 - Sine on Front panel keyboard failed

11801 - Init of I2C failed

11802 - The muting of the Audio failed

11803 - The un-mute of the Audio failed

11804 - The selection of the clock source failed

11805 - Error cannot start VSM audio in port

11901 - Init of I2C failed

11902 - The muting of the Audio failed

11903 - The un-mute of the Audio failed

11904 - The selection of the clock source failed

11905 - Error cannot start VSM Audio in port

12001 - Invalid input

12201 - I2C bus busy before start

12202 - NVRAM access time-out

12203 - No NVRAM acknowledgement

12204 - NVRAM time-out

12205 - NVRAM Write/Read back failed

12301 - I2C bus busy before start

12302 - NVRAM read access time-out

12303 - No NVRAM read acknowledgement

12304 - NVRAM read failed

13000 - Bootcode application version boot version

13001 - Can not find version in FLASH.

13100 - Recorder application version: recorder version

13101 - Can not find version in FLASH.

13200 - Diagnostics application version: diagversion

13201 - Can not find version in FLASH.

13300 - Download application version: download version

13301 - Can not find version in FLASH.

13701 - Turning off Macrovision failed

20001 - I2C bus busy before start

20002 - Video Encoder access time-out

20003 - No acknowledgement from Video Encoder

20004 - No data send/received to or from Video Encoder

20005 - SAA7118 VIP can not be initialized

20201 - I2C bus busy before start

20202 - SAA7118 VIP access time-out

20203 - No acknowledgement from SAA7118 VIP

20204 - No data received from SAA7118 VIP

20301 - Error audio encoder SRAM access cannot initialize I2C

20302 - Error audio encoder SRAM access cannot reset DSP through I2C

20303 - Error audio encoder SRAM access cannot download boot

20304 - Error audio encoder cannot download test code

20305 - Error audio encoder cannot obtain result of test

20306 - Error audio encoder SRAM access stuck-at-zero data line

20307 - Error audio encoder SRAM access stuck-at-one data line

20308 - Error audio encoder SRAM access stuck-at-one address line

20309 - Error audio encoder SRAM access address line. Address line x is connected to data line y

20310 - Error audio encoder SRAM access address lines address line x and address line y are connected

20311 - Error audio encoder SRAM access data lines data line x and data line y are connected

20312 - Error audio encoder SRAM access illegal data received

20401 - Error audio encoder access cannot initialize I2C

20402 - Error audio encoder access cannot reset DSP through I2C

20403 - Error audio encoder accessing ICR register

20404 - Error audio encoder access stuck-at-zero of data line

20405 - Error audio encoder access stuck-at-one of data line

20406 - Audio encoder access data lines data line x and data line y are interconnected

20501 - Error audio encoder SRAM WRR cannot initialize I2C

20502 - Error audio encoder SRAM WRR cannot reset DSP through I2C

20503 - Error audio encoder WRR cannot down-

load boot

20504 - Error audio encoder cannot download test code

20505 - Error audio encoder SRAM WRR cannot obtain result of test

20506 - Error audio encoder WRR SRAM stuck-at-zero data bit

20507 - Error audio encoder WRR SRAM stuck-at-one data bit

20508 - Error audio encoder WRR SRAM data lines data line x and data line y are connected

20509 - Error audio encoder WRR SRAM illegal data received

20601 - Error audio encoder interrupt cannot initialize I2C

20602 - Error audio encoder interrupt cannot reset DSP through I2C

20603 - Error audio encoder cannot download test code

20604 - Error occurred accessing VSM

20605 - Audio encoder interrupt not received

20606 - Error occurred while activating the encoder

20607 - Error audio encoder interrupt cannot initialize empress

20608 - Error occurred while getting interrupt reason

20701 - Error audio encoder I2C cannot reset DSP through I2C

20702 - Error audio encoder cannot download boot

20703 - Error audio encoder cannot download TEST code

20704 - Error audio encoder I2C bus busy

20705 - Error audio encoder I2C cannot write slave address

20706 - Error audio encoder I2C no acknowledgement received

20707 - Error audio encoder I2C cannot send/receive data

20708 - Error audio encoder received data through I2C was invalid

20801 - I2C access failed.

20802 - SAA7118 VIP can not be initialized.

20803 - Invalid input

20900 - B1. B2. B3. B4. B5. B6. B7. B8. B9. B10. B11. B12.

20901 - Firmware download of EMPRESS failed

20902 - I2C bus busy before start

20903 - EMPRESS access time-out

20904 - No acknowledgement from the EMPRESS

20905 - No data send to the EMPRESS

20906 - No data received from the EMPRESS

30001 - VSM SDRAM Bank1 Memory data bus test fails.

30002 - VSM SDRAM Bank1 Memory address bus test fails.

30003 - VSM SDRAM Bank1 Physical memory device test fails.

30004 - VSM SDRAM Bank2 Memory data bus test fails.

30005 - VSM SDRAM Bank2 Memory address bus test fails.

30006 - VSM SDRAM Bank2 Physical memory device test fails.

30007 - VSM SDRAM Bank1 VSM interrupt register A has a-stuck at- error for value:

30008 - VSM SDRAM Bank2 VSM interrupt register A has a-stuck at- error for value:

30101 - VSM SDRAM Bank1 Memory data bus test fails.

30102 - VSM SDRAM Bank1 Memory address bus test fails.

30103 - VSM SDRAM Bank1 Physical memory device test fails.

30104 - VSM SDRAM Bank2 Memory data bus test fails.

30105 - VSM SDRAM Bank2 Memory address bus test fails.

30106 - VSM SDRAM Bank2 Physical memory device test fails.

30201 - VSM SDRAM Bank1 Memory data bus test fails.

30202 - VSM SDRAM Bank1 Memory address bus test fails.

30203 - VSM SDRAM Bank1 Physical memory device test fails.

30204 - VSM SDRAM Bank2 Memory bus test wrong.

30205 - VSM SDRAM Bank2 Memory address bus test fails.

30206 - VSM SDRAM Bank2 Physical memory device test fails.

30301 - VSM interrupt register A has a -stuck at- error for value:

30302 - VSM interrupt register B has a -stuck at- error for value:

30303 - Interrupt A wasn't raised.

30304 - Interrupt B wasn't raised.

30305 - Interrupts A and B were raised.

30401 - VSM SDRAM Bank1 Memory data bus test fails.

30402 - VSM SDRAM Bank1 Memory address bus test fails.

30403 - VSM SDRAM Bank1 Physical memory device test fails.

30404 - VSM SDRAM Bank2 Memory data bus test fails.

30405 - VSM SDRAM Bank2 Memory address bus test fails.

30406 - VSM SDRAM Bank2 Physical memory device test fails.

30501 - Communication with the Analog Board fails.

30502 - Echo test to Analog Board returned wrong string.

40001 - NVRAM Reset; I2C failed

40100 - NVRAM address = 0xaddress -> Bytevalue = 0xvalue

40101 - NVRAM Read; I2C failed

40102 - NVRAM Read; Invalid input

40201 - NVRAM Modify; I2C failed

40202 - NVRAM Modify; Invalid input

40300 - DV Unique ID = id

40301 - NVRAM Read DV Unique ID; I2C failed

40400 - \r\n Error log: \r\n error String \r\n Ö

40401 - NVRAM error log; I2C failed

40402 - NVRAM error log is invalid

40403 - Front panel failed

40701 - NVRAM error log reset; I2C failed

40900 - Region code Change counter is reset

40901 - NVRAM region code reset; I2C failed

41001 - NVRAM Store DV Unique ID; I2C failed

41002 - NVRAM Store DV Unique ID; Invalid input

50007 - Execution of the command on the Analog Board failed.

50008 - The front panel could not be accessed by the Analog Board.

50009 - The echo from the front panel processor was not correct.

50100 - Front panel version: FP version

50102 - Execution of the command on the Analog Board failed.

50103 - The front panel could not be accessed by the Analog Board.

50204 - Execution of the command on the Analog Board failed.

50205 - The front panel could not be accessed by the Analog Board.

50206 - The front panel did not show a starburst.

50207 - The user skipped the FP-which pattern test.

50208 - The user returned an unknown confirmation: confirmation

50209 - The front panel did not show horizontal segments.

50210 - The front panel did not show vertical segments.

50304 - Execution of the command on the Analog Board failed.

50305 - The front panel could not be accessed by the Analog Board.

50306 - The front panel did not light all labels.

50307 - The user skipped the rest of the FP-label test.

50308 - The user returned an unknown confirmation: confirmation

50404 - Execution of the command on the Analog Board failed.

50405 - The front panel could not be accessed by the Analog Board.

50406 - The LED’s could not be turned on.

50407 - The user skipped the rest of the FP-LED test.

50408 - The user returned an unknown confirmation: confirmation

50502 - Front panel Keyboard; test failed

50503 - Front panel Keyboard; test aborted

50504 - Front panel Keyboard; not all keys were pressed

50505 - Front panel keyboard I2C connection failed

50506 - Unable to get slash version

50602 - Front panel Remote control; test failed

50603 - Front panel Remote control; test aborted

50604 - Front panel remote control; can not access FP

50605 - Front panel remote control; no user input received

50701 - Execution of the command on the Analog Board failed.

50702 - The front panel could not be accessed by the Analog Board.

50703 - The front panel did not show a starburst.

50704 - The user skipped the FP-starburst test.

50705 - The user returned an unknown confirmation: confirmation

50801 - Execution of the command on the Analog Board failed.

50802 - The front panel could not be accessed by the Analog Board.

50803 - The front panel did not show vertical segments.

50804 - The user skipped the FP-vertical segments test.

50805 - The user returned an unknown confirmation: confirmation

50901 - Execution of the command on the Analog Board failed.

50902 - The front panel could not be accessed by the Analog Board.

50903 - The front panel did not show horizontal segments.

50904 - The user skipped the FP-horizontal segments test.

50905 - The user returned an unknown confirmation: confirmation

51401 - Execution of the command on the Analog Board failed.

51402 - The front panel could not be accessed by the Analog Board.

51403 - The beeper did not sound.

51404 - The user skipped the FP-Beep test.

51405 - The user returned an unknown confirmation: confirmation

51501 - Execution of the command on the Analog Board failed.

51502 - The front panel could not be accessed by the Analog Board.

51503 - The disc bar did not display properly.

51504 - The user skipped the disc bar test.

51505 - The user returned an unknown confirmation: confirmation

51601 - Execution of the command on the Analog Board failed.

51602 - The front panel could not be accessed by the Analog Board.

51603 - The disc bar dots did not display properly.

51604 - The user skipped the disc bar dots test.

51605 - The user returned an unknown confirmation: confirmation

51701 - Execution of the command on the Analog Board failed.

51702 - The front panel could not be accessed by the Analog Board.

51703 - The VU grid did not display properly.

51704 - The user skipped the VU grid test.

51705 - The user returned an unknown confirmation: confirmation

51801 - Execution of the command on the Analog Board failed.

51802 - The front panel could not be accessed by the Analog Board.

51803 - The front panel could not be dimmed.

51804 - The user skipped the FP-Dim test.

51805 - The user returned an unknown confirmation: confirmation

51901 - Execution of the command on the Analog Board failed.

51902 - The front panel could not be accessed by the Analog Board.

51903 - The front panel did not show segments blinking.

51904 - The user skipped the FP-blinking test.

51905 - The user returned an unknown confirmation: confirmation

52001 - Execution of the command on the Analog Board failed.

52002 - The front panel could not be accessed by the Analog Board.

52003 - The front panel did not show all segments lit.

52004 - The user skipped the FP-light all segments test.

52005 - The user returned an unknown confirmation: confirmation

52201 - Communication with Analog Board fails.

52202 - front panel can not be accessed by the Analog Board.

52301 - Communication with Analog Board fails.

52302 - front panel can not be accessed by the Analog Board.

60101 - Basic Engine returned error number 0x error number

60102 - Parity error from Basic Engine to Serial

60103 - Communication time-out error

60104 - Unexpected response from Basic Engine

60105 - Echo loop could not be closed

60106 - Wrong echo pattern received

60200 - Version: nr1.nr2.nr3

60201 - Basic Engine returned error number 0xerrornumber

60202 - Parity error from Basic Engine to Serial

60203 - Communication time-out error

60204 - Unexpected response from Basic Engine

60205 - Front Panel failed.

60301 - Basic-Engine time-out error

60401 - Basic Engine returned error number 0xerrornumber

60402 - Parity error from Basic Engine to Serial

60403 - Communication time-out error

60404 - Unexpected response from Basic Engine

60405 - Focus loop could not be closed

60501 - Basic Engine returned error number 0xerrornumber

60502 - Parity error from Basic Engine to Serial

60503 - Communication time-out error

60504 - Unexpected response from Basic Engine

60601 - Basic Engine returned error number 0xerrornumber

60602 - Parity error from Basic Engine to Serial

60603 - Communication time-out error

60604 - Unexpected response from Basic Engine

60701 - Basic Engine returned error number 0xerrornumber

60702 - Parity error from Basic Engine to Serial

60703 - Communication time-out error

60704 - Unexpected response from Basic Engine

60801 - Basic Engine returned error number 0xerrornumber

60802 - Parity error from Basic Engine to Serial

60803 - Communication time-out error

60804 - Unexpected response from Basic Engine

60805 - Radial loop could not be closed

60901 - Basic Engine returned error number 0xerrornumber

60902 - Parity error from Basic Engine to Serial

60903 - Communication time-out error

60904 - Unexpected response from Basic Engine

61501 - Basic Engine returned error number 0xerrornumber

61502 - Parity error from Basic Engine to Serial

61503 - Communication time-out error

61504 - Unexpected response from Basic Engine

61601 - Basic Engine returned error number 0xerrornumber

61602 - Parity error from Basic Engine to Serial

61603 - Communication time-out error

61604 - Unexpected response from Basic Engine

61701 - BE tray-in command failed

61702 - BE read-TOC command failed

61703 - BE VSM interrupt initialization failed

61704 - BE set IRQ command failed

61705 - BE no disc or wrong disc inserted

61706 - BE rec-pause command failed

61707 - BE VSM BE out DMA initialization failed

61708 - BE VSM BE out initialization failed

61709 - BE VSM BE out DMA start failed

61710 - BE VSM BE out start failed

61711 - BE rec command failed

61712 - BE VSM out under run error occurred

61713 - BE record complete interrupt not raised

61714 - BE get IRQ command failed

61715 - BE no interrupt was raised by BE

61716 - BE VSM DMA out not finished

61717 - BE stop command after writing failed

61718 - BE VSM Sector processor initialization failed

61719 - BE VSM sector processor DMA initialization failed

61720 - BE VSM sector processor DMA start failed

61721 - BE VSM sector processor start failed

61722 - BE seek command failed

61723 - BE VSM sector processor error occurred

61724 - BE read timeout occurred

61725 - BE stop command after reading failed

61726 - BE difference found in data at disc sector 0xdiscsector

61727 - This nucleus cannot be executed because the Self-Test failed

61801 - BE I2C initialization failed

61802 - This nucleus cannot be executed because the Self-Test failed

61901 - The Self Test failed with result: 0xnr1 0xnr20xnr3

61902 - Basic Engine returned error number 0xerrornumber

61903 - Parity error from Basic Engine to Serial

61904 - Communication time-out error

61905 - Unexpected response from Basic Engine

62001 - Self-Test: errorstring1 Laser-Test: errorstring2 Spindle M-Test: errorstring3 Sledge M-Test: error string4 Focus-Test: errorstring5

62100 - The forward sense level is 0xlevel

62101 - Basic Engine returned error number 0xerrornumber

62102 - Parity error from Basic Engine to Serial

62103 - Communication time-out error

62104 - Unexpected response from Basic Engine

62201 - The BE-self-diagnostic-spindle-motor-test failed

62202 - Basic Engine returned error number 0xerrornumber

62203 - Parity error from Basic Engine to Serial

62204 - Communication time-out error

62205 - Unexpected response from Basic Engine

62301 - The BE-focus-test failed

62302 - Basic Engine returned error number 0xerrornumber

62303 - Parity error from Basic Engine to Serial

62304 - Communication time-out error

62305 - Unexpected response from Basic Engine

62401 - The BE-self-diagnostic-sledge-motor-test failed

62402 - Basic Engine returned error number 0xerrornumber

62403 - Parity error from Basic Engine to Serial

62404 - Communication time-out error

62405 - Unexpected response from Basic Engine

62700 - BE EEPROM address = address -> Byte value = 0xvalue

62701 - Basic Engine returned error number

0xerrornumber

62702 - Parity error from Basic Engine to Serial

62703 - Communication time-out error

62704 - Unexpected response from Basic Engine

62705 - BE read EEPROM; invalid input

62801 - Basic Engine returned error number 0xerrornumber

62802 - Parity error from Basic Engine to Serial

62803 - Communication time-out error

62804 - Unexpected response from Basic Engine

62805 - BE write EEPROM; invalid input

62901 - Basic Engine returned error number 0xerrornumber

62902 - Parity error from Basic Engine to Serial

62903 - Communication time-out error

62904 - Unexpected response from Basic Engine

62905 - Radial loop could not be closed

63001 - Basic Engine returned error number 0xerrornumber

63002 - Parity error from Basic Engine to Serial

63003 - Communication time-out error

63004 - Unexpected response from Basic Engine

63100 - Number of times Tray went Open/Closed: nr1 Total hours the CD laser was on: nr2 Total hours the DVD laser was on: nr3 Total hours the write laser was on: nr4

63101 - Basic Engine returned error number 0xerrornumber

63102 - Parity error from Basic Engine to Serial

63103 - Communication time-out error

63104 - Unexpected response from Basic Engine

63201 - Basic Engine returned error number 0xerrornumber

63202 - Parity error from Basic Engine to Serial

63203 - Communication time-out error

63204 - Unexpected response from Basic Engine

63300 - Momentary errors (Byte 1 - Byte 7): 0xb1 0xb2 0xb30xb4 0xb5 0xb6 0xb7 Cumulative errors (Byte 1 - Byte 7): 0xb10xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Fatal errors (Oldest - Youngest): 0xb1 0xb2 0xb3 0xb4 0xb5

63301 - Basic Engine returned error number 0xerrornumber

63302 - Parity error from Basic Engine to Serial

63303 - Communication time-out error

63304 - Unexpected response from Basic Engine

63401 - Basic Engine returned error number 0xerrornumber

63402 - Parity error from Basic Engine to Serial

63403 - Communication time-out error

63404 - Unexpected response from Basic Engine

63501 - Basic Engine returned error number 0xerrornumber

63502 - Parity error from Basic Engine to Serial

63503 - Communication time-out error

63504 - Unexpected response from Basic Engine

63505 - Error string Ö The basic engine will reject all player commands

63901 - Basic Engine returned error number 0xerrornumber

63902 - Parity error from Basic Engine to Serial

63903 - Communication time-out error

63904 - Unexpected response from Basic Engine

64000 - BE OPU number = opu number

64001 - Basic Engine returned error number 0xerrornumber

64002 - Parity error from Basic Engine to Serial

64003 - Communication time-out error

64004 - Unexpected response from Basic Engine

64100 - The data was successfully written on and read from a DVD disc

64101 - The tray-in command failed

64102 - The read-TOC command failed

64103 - The VSM interrupt initialization failed

64104 - The set IRQ command failed

64105 - No disc or wrong disc inserted

64106 - The rec-pause command failed

64107 - The VSM BE out DMA initialization failed

64108 - The VSM BE out initialization failed

64109 - The VSM BE out DMA start failed

64110 - The VSM BE out start failed

64111 - The rec command failed

64112 - The VSM out under run error occurred

64113 - The record complete interrupt was not raised

64114 - The get IRQ command failed

64115 - There was no interrupt raised by BE

64116 - The VSM DMA did not finished

64117 - The stop command after writing failed

64118 - The VSM Sector processor initialization failed

64119 - The VSM sector processor DMA initialization failed

64120 - The VSM sector processor DMA start failed

64121 - The VSM sector processor start failed

64122 -
The seek command failed

64123 - The VSM sector processor error occurred

64124 - The read timeout occurred

64125 - The stop command after reading failed

64126 - There was a difference found in data at a specific disc sector

64127 - The result of the self test contains errors

64128 - An error interrupt was raised by BE

64129 - The calibrate-record command failed

64130 - To many retries

64131 - BE update RAI command after writing failed

64132 - BE find first recordable address command failed

64133 - DVD+R disc is full

64201 - BE i2c initialization failed

64202 - This nucleus cannot be executed because the Self-Test failed

70000 - Echo test OK

70001 - Echo test returned wrong string.

70002 - Communication with Analog Board fails

70300 - Software Version

70301 - Can not find segment in FLASH ROM on the Analog Board

70302 - Communication with Analog Board fails

70400 - Hardware Version

70401 - Can not find segment in FLASH ROM on the Analog Board

70402 - Communication with Analog Board fails

70500 - Clock adjusted OK

70501 - Can not adjust the clock on the Analog Board.

70502 - Wrong date/time text size.

70503 - Communication with Analog Board fails

70600 - Tuner accessibility test OK

70601 - Can not access Tuner on the Analog Board.

70602 - Communication with Analog Board fails

70700 - Frequency download OK

70701 - Wrong frequency table size.

70702 - Can not download the frequency table into the Analog NVRAM.

70703 - Can not download the frequency table into the Analog NVRAM.

70704 - Communication with Analog Board fails

70800 - Data Slicer test OK

70801 - Test of the Data Slicer on the Analog Board fails.

70802 - Communication with Analog Board fails

70900 - Sound Processor test OK

70901 - Test of the Sound Processor on the Analog Board fails.

70902 - Communication with Analog Board fails

71000 - AV Selector test OK

71001 - Test of the AV Selector on the Analog Board fails.

71002 - Communication with Analog Board fails

71100 - NVRAM test OK

71101 - Test of the NVRAM on the Analog Board fails.

71102 - Communication with Analog Board fails

71200 - Video routing on the Analog Board OK

71201 - Routing the Video on the Analog Board fails.

71202 - Invalid input.

71203 - Communication with Analog Board fails

71300 - Audio routing on the Analog Board OK

71301 - Routing the Audio on the Analog Board fails.

71302 - Invalid input.

71303 - Communication with Analog Board fails

71501 - Invalid slash version, default slash version is set.

71502 - Setting the slash version on the Analog Board fails.

71503 - Communication with Analog Board fails

71600 - Application Version

71601 - Can not find segment in FLASH ROM on the Analog Board

71602 - Communication with Analog Board fails

71700 - Diagnostics Version

71701 - Can not find segment in FLASH ROM on the Analog Board

71702 - Communication with Analog Board fails

71800 - Download Version

71801 - Can not find segment in FLASH ROM on the Analog Board

71802 - Communication with Analog Board fails

72001 - Adjusting BarGraph Level failed

72002 - Communication with Analog Board fails

72101 - Storing clock correction failed

72102 - Value out of range: default value stored

72103 - Invalid input.

72104 - Communication with Analog Board fails

72201 - Initializing the 1Hz signal on the Clock IC failed

72202 - Communication with Analog Board fails

72301 - Clearing the NVRAM on the Analog Board fails

72302 - Communication with Analog Board fails

72400 - Segment checksum is: checksum which is correct for every segment

72401 - Segment could not be found or segment checksum is: checksum C, however it should be: checksum E for every segment

72402 - Communication with Analog Board fails

72900 - Date received

72901 - Data returned

72902 - Communication on I2C-bus failed on the Analog Board fails.

72903 - Communication with Analog Board fails

73001 - Storing the external presets on the Analog Board fails

73002 - Communication with Analog Board fails

73100 - 0xslash version where slash version is the slash version read from the Analog Board

73101 - Error while reading out slash version.

73102 - I2C Write error.

73103 - I2C Read error.

73104 - Communication with Analog Board fails

73201 - Storing the Reference Voltage for the Tuner failed

73202 - Invalid input.

73203 - Communication with Analog Board fails

80000 - The DVIO module is present in the system.

80001 - The DVIO module is not present in the system.

80100 - The DVIO module has been reset OK.

80101 - The DVIO module is not present in the system.

80102 - The DVIO module could not be reset.

80103 - Could not initialize I2C before Reset.

80200 - The accessibility of the DVIO module is OK.

80201 - The DVIO Board is not present in this DVDR.

80202 - Could not initialize I2C.

80203 - Unable to reset the DVIO module.

80204 - Unable to receive the reset indication from the DVIO module.

80205 - Unable to send the configuration to the DVIO module.

80206 - Unable to download the chip ID to the DVIO module.

80207 - Unable to set the mode of the DVIO module to IDLE.

80208 - Software Error in function Handle State Awaiting Reply!!

80209 - Maximal number of retries reached by Handle State Sending!!

80210 - Maximal number of retries (NACKs) reached (Handle State Sending)

80211 - We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!

80212 - We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!

80213 - We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!

80214 - VSM UART error timeout transmitting command

80215 - VSM UART error timeout receiving reply

80216 - VSM UART frame error occurred receiving from DVIO Board

80217 - VSM UART parity error occurred receiving from DVIO Board

80218 - The confirmation/indication from the DVIO module is invalid.

80300 - The accessibility of the DVIO module is OK.

80301 - The DVIO Board is not present in this DVDR.

80302 - Could not initialize I2C.

80303 - Unable to reset the DVIO module.

80304 - Unable to receive the reset indication from the DVIO module.

80305 - Unable to send the configuration to the DVIO module.

80306 - Unable to download the chip ID to the DVIO module.

80307 - Unable to set the mode of the DVIO module to IDLE.

80308 - Software Error in function Handle State Awaiting Reply!!

80309 - Maximal number of retries reached by Handle State Sending!!

80310 - Maximal number of retries (NACKs) reached (Handle State Sending)

80311 - We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!

80312 - We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!

80313 - We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!

80314 - VSM UART error timeout transmitting command

80315 - VSM UART error timeout receiving reply

80316 - VSM UART frame error occurred receiving from DVIO Board

80317 - VSM UART parity error occurred receiving from DVIO Board

80318 - The confirmation/indication from the DVIO module is invalid.

80400 - The accessibility of the DVIO module is OK.

80401 - The DVIO Board is not present in this DVDR.

80402 - Could not initialize I2C.

80403 - Unable to reset the DVIO module.

80404 - Unable to receive the reset indication from the DVIO module.

80405 - Unable to send the configuration to the DVIO module.

80406 - Unable to download the chip ID to the DVIO module.

80407 - Unable to set the mode of the DVIO module to IDLE.

80408 - Software Error in function Handle State Awaiting Reply!!

80409 - Maximal number of retries reached by Handle State Sending!!

80410 - Maximal number of retries (NACKs) reached (Handle State Sending)

80411 - We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!

80412 - We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!

80413 - We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!

80414 - VSM UART error timeout transmitting command

80415 - VSM UART error timeout receiving reply

80416 - VSM UART frame error occurred receiving from DVIO Board

80417 - VSM UART parity error occurred receiving from DVIO Board

80418 - The confirmation/indication from the DVIO module is invalid.

80501 - The DVIO Board is not present in this DVDR.

80502 - The I2C could not be initialized.

80503 - The DVIO module could not be reset.

80504 - Unable to receive the reset indication from the DVIO module.

80505 - Unable to send the configuration to the DVIO module.

80506 - Unable to download the chip ID to the DVIO module.

80507 - Unable to set the mode of the DVIO module to IDLE.

80508 - Software Error in Handle State Awaiting Reply function!

80509 - Maximal number of retries reached by Handle State Sending!

80510 - Maximal number of retries (NACKs) reached (Handle State Sending)

80511 - We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!

80512 - We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!

80513 - We tried to receive an Acknowledgement for DVIO_MAX_RETRIES_ACK times

80514 - VSM UART error timeout transmitting command

80515 - VSM UART error timeout receiving reply

80516 - VSM UART frame error occurred receiving from DVIO Board

80517 - VSM UART parity error occurred receiving from DVIO Board

80518 - The confirmation/indication from the DVIO module is invalid.

80519 - Setting the DVIO module in/out diagnostics mode failed

80520 - Invalid input

80521 - Getting the errors of the self-test failed

80522 - Self-test failed

80601 - The DVIO Board is not present in this DVDR.

80602 - The I2C could not be initialized.

80603 - The DVIO module could not be reset.

80604 - Unable to receive the reset indication from the DVIO module.

80605 - Unable to send the configuration to the DVIO module.

80606 - Unable to download the chip ID to the DVIO module.

80607 - Unable to set the mode of the DVIO module to IDLE.

80608 - Software Error in Handle State Awaiting Reply function!

80609 - Maximal number of retries reached by Handle State Sending!

80610 - Maximal number of retries (NACKs) reached (Handle State Sending)

80611 - We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!

80612 - We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!

80613 - We tried to receive an Acknowledgement for DVIO_MAX_RETRIES_ACK times!

80614 - VSM UART error timeout transmitting command

80615 - VSM UART error timeout receiving reply

80616 - VSM UART frame error occurred receiving from DVIO Board

80617 - VSM UART parity error occurred receiving from DVIO Board

80618 - The confirmation/indication from the DVIO module is invalid.

80619 - Setting the DVIO module in/out diagnostics mode failed

80701 - The DVIO Board is not present in this DVDR.

80702 - The I2C could not be initialized.

80703 - The DVIO module could not be reset.

80704 - Unable to receive the reset indication from the DVIO module.

80705 - Unable to send the configuration to the DVIO module.

80706 - Unable to download the chip ID to the DVIO module.

80707 - Unable to set the mode of the DVIO module to IDLE.

80708 - Software Error in Handle State Awaiting Reply function!

80709 - Maximal number of retries reached by Handle State Sending!

80710 - Maximal number of retries (NACKs) reached (Handle State Sending)

80711 - We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!

80712 - We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!

80713 - We tried to receive an Acknowledgement for DVIO_MAX_RETRIES_ACK times!

80714 - VSM UART error timeout transmitting command

80715 - VSM UART error timeout receiving reply

80716 - VSM UART frame error occurred receiving from DVIO Board

80717 - VSM UART parity error occurred receiving from DVIO Board

80718 - The confirmation/indication from the DVIO module is invalid.

80719 - Setting the DVIO module in/out diagnostics mode failed

90121 - Error: Audio data in host memory contains wrong frequency: frequency Hz

90122 - Error: Audio data in host memory contains silence!

90123 - There is no correct audio frame in the buffer

90124 - The audio frame has an illegal version bit

90125 - The audio frame has an illegal bitrate-index

90126 - The audio frame has an illegal sampling rate

90127 - The CRC of the audio frame is wrong

90128 - The audio frame is not MPEG-I layer II !

90129 - Error cannot de-mute DAC on Analog Board

90201 - Initialization of I2C failed

90202 - Initialization of VIP and EMPIRE failed

90203 - Initialization of PLL / Link failed.

90204 - Next descriptor address set wrong.

90205 - Turning on the colorbar failed

90206 - No I2C communication possible to start video encoder.

90207 - Starting the video encoder failed.

90208 - Transfer of data from video encoder to VSM failed.

90209 - Stopping the encoder failed.

90210 - Turning off the colorbar failed.

90211 - Cannot initialize hostdecoder parallel

input

90212 - Cannot Initialize VSM AV-out DMA port

90213 - Cannot Initialize VSM AV-out port

90214 - Cannot start VSM AV-out DMA port

90215 - Cannot start VSM AV-out port

90216 - Transfer of data from VSM to host decoder failed.

90217 - VSM and Hostdec memory do not match (compared after transfer)

90218 - Decoding of the Video data in the host decoder memory failed

90219 - The data in the host decoder is not equal to a colorbar

90220 - The video encoder did not return the Group Of Picture count.

90221 - The video encoder did not receive data from the VIP.

90223 - Initialization of VIP and EMPRESS failed

90224 - The video encoder did not return the current status.

90225 - The video encoder timed out in BUSY mode. (No VIP input)

90226 - The video encoder did not return the current bit rate.

90227 - The video encoder did not switch to ENCODING mode.

90228 - The video encoder could not start from STOP/IDLE mode.

90229 - The video encoder did not switch from IDLE to STOP mode.

90301 - Initialization of I2C failed

90302 - I2C communication to VIP failed

90303 - Initialization of VIP failed

90304 - Generation of Close Caption data failed

90305 - VIP not locked to Video signal

90306 - Initialization of VBI Extractor failed

90307 - No CC data received

90308 - Closed Caption data overrun

90309 - Closed Caption data does not match

90310 - Switch off colorbar failed

90401 - Initialization of I2C failed

90402 - Initialization of VIP and EMPIRE failed

90403 - Initialization of PLL / Link failed.

90404 - Next descriptor address set wrong.

90405 - Turning on the colorbar failed

90406 - No I2C communication possible to start video encoder.

90407 - Starting the video encoder failed.

90408 - Transfer of data from video encoder to VSM failed.

90409 - Stopping the encoder failed.

90410 - Turning off the colorbar failed.

90411 - Cannot initialize host decoder parallel input

90412 - Cannot Initialize VSM AV-out DMA port

90413 - Cannot Initialize VSM AV-out port

90414 - Cannot start VSM AV-out DMA port

90415 - Cannot start VSM AV-out port

90416 - Transfer of data from VSM to host decoder failed.

90417 - VSM and Hostdec memory do not match (compared after transfer)

90418 - Decoding of the video data in the host decoder memory failed

90419 - The data in the host decoder is not equal to a colorbar

90420 - The video encoder did not return the Group Of Picture count.

90421 - The video encoder did not receive data from the VIP.

90422 - Execution of the command on the Analog Board failed.

90423 - Initialization of VIP and EMPRESS failed

90424 - The video encoder did not return the current status.

90425 - The video encoder timed out in BUSY mode. (no VIP input)

90426 - The video encoder did not return the current bit rate.

90427 - The video encoder did not switch to ENCODING mode.

90428 - The video encoder could not start from STOP/IDLE mode.

90429 - The video encoder did not switch from IDLE to STOP mode.

90501 - Initialization of I2C failed

90502 - I2C communication to VIP failed

90503 - Initialization of VIP failed

90504 - Generation of Close Caption data failed

90505 - VIP not locked to Video signal

90506 - Initialization of VBI Extractor failed

90507 - No CC data received

90508 - Closed Caption data overrun

90509 - Closed Caption data does not match

90510 - Switch off colorbar failed

90511 - Execution of the command on the Analog Board failed.

90601 - Initialization of I2C failed

90602 - Initialization of VIP and EMPIRE failed

90603 - Initialization of PLL / Link failed.

90604 - Next descriptor address set wrong.

90605 - Turning on the colorbar failed

90606 - No I2C communication possible to start video encoder.

90607 - Starting the video encoder failed.

90608 - Transfer of data from video encoder to VSM failed.

90609 - Stopping the encoder failed.

90610 - Turning off the color bar failed.

90611 - Cannot initialize host decoder parallel input

90612 - Cannot initialize VSM AV-out DMA port

90613 - Cannot initialize VSM AV-out port

90614 - Cannot start VSM AV-out DMA port

90615 - Cannot start VSM AV-out port

90616 - Transfer of data from VSM to host

decoder failed.

90617 - VSM and Hostdec memory do not match (compared after transfer)

90618 - Decoding of the Video data in the host decoder memory failed

90619 - The data in the host decoder is not equal to a colorbar

90620 - The video encoder did not return the Group Of Picture count.

90621 - The video encoder did not receive data from the VIP.

90622 - Execution of the command on the Analog Board failed.

90623 - Initialization of VIP and EMPRESS failed

90624 - The video encoder did not return the current status.

90625 - The video encoder timed out in BUSY mode. (no VIP input)

90626 - The video encoder did not return the current bit rate.

90627 - The video encoder did not switch to ENCODING mode.

90628 - The video encoder could not start from STOP/IDLE mode.

90629 - The video encoder did not switch from IDLE to STOP mode.

90701 - Initialization of I2C failed

90702 - I2C communication to VIP failed

90703 - Initialization of VIP failed

90704 - Generation of Close Caption data failed

90705 - VIP not locked to Video signal

90706 - Initialization of VBI Extractor failed

90707 - No CC data received

90708 - Closed Caption data overrun

90709 - Closed Caption data does not match

90710 - Switch off colorbar failed

90711 - Execution of the command on the Analog Board failed.

90801 - Error routing the Audio back to the Digital Board.

90802 - Error cannot initialize I2C

90803 - Error cannot initialize VIP

90804 - Error cannot set ADC enable pin

90805 - Error cannot set VSM audio clock

90806 - Error preparing the 12kHz audio-sine

90807 - Error cannot initialize audio encoder

90808 - Error cannot initialize VSM audio in port

90809 - Error cannot initialize VSM audio in DMA port

90810 -Error cannot initialize VSM audio out DMA port

90811 - Error cannot initialize audio VSM out port

90812 - Error cannot initialize host decoder audio in

90813 - Error loop audio user/dealer cannot start audio encoder

90814 - Error cannot start VSM audio in DMA port

90815 - Error starting the 12 kHz Audio-sine

90816 - Error transfer data from audio encoder to VSM

90817 - Error cannot start VSM AV out DMA port

90818 - Error cannot start VSM AV out port

90819 - Error transfer data from VSM to host decoder

90820 - Error: audio data in host memory and VSM memory differ

90821 - Error: audio data in host memory contains wrong frequency: frequency Hz

90822 - Error: audio data in host memory contains silence!

90823 - There is no correct audio frame in the buffer

90824 - The audio frame has an illegal version bit

90825 - The audio frame has an illegal bit rate-index

90826 - The audio frame has an illegal sampling rate

90827 - The CRC of the audio frame is wrong

90828 - The audio frame is not MPEG-I layer II!

90829 - Error cannot de-mute DAC on Analog Board

90901 - Error routing the Audio back to the Digital Board.

90902 - Error cannot initialize I2C

90903 - Error cannot initialize VIP

90904 - Error cannot set ADC enable pin

90905 - Error cannot set VSM audio clock

90906 - Error preparing the 12kHz audio-sine

90907 - Error cannot initialize audio encoder

90908 - Error cannot initialize VSM audio in port

90909 - Error cannot initialize VSM audio in DMA port

90910 - Error cannot initialize VSM audio out DMA port

90911 - Error cannot initialize audio VSM out port

90912 - Error cannot initialize host decoder audio in

90913 - Error loop audio user/dealer cannot start audio encoder

90914 - Error cannot start VSM audio in DMA port

90915 - Error starting the 12kHz audio-sine

90916 - Error transfer data from audio encoder to VSM

90917 - Error cannot start VSM AV out DMA port

90918 - Error cannot start VSM AV out port

90919 - Error transfer data from VSM to host decoder

90920 - Error: Audio data in host memory and VSM memory differ

90921 - Error: Audio data in host memory contains wrong frequency: frequency Hz

90922 - Error: Audio data in host memory contains silence!

90923 - There is no correct audio frame in the buffer

90924 - The audio frame has an illegal version bit

90925 - The audio frame has an illegal bitrate-index

90926 - The audio frame has an illegal sampling

rate

90927 - The CRC of the audio frame is wrong

90928 - The audio frame is not MPEG-I layer II !

90929 - Error cannot de-mute DAC on Analog Board

140001 - I2C to Clock failed or I2C Initialization failed
140101 - I2C to Clock failed or I2C Initialization failed

141201 - Progressive Scan Board I2C bus busy

141211 - Progressive Scan Board I2C FLI2200 bus busy

141212 - Progressive Scan Board I2C FLI2200 read access time-out

141213 - Progressive Scan Board I2C FLI2200 no read acknowledgement

141214 - Progressive Scan Board I2C FLI2200 read failed

141215 - Progressive Scan Board I2C FLI2200 write access time-out

141216 - Progressive Scan Board I2C FLI2200 no write acknowledgement

141217 - Progressive Scan Board I2C FLI2200 write failed

141218 - Progressive Scan Board I2C FLI2200 failed

141221 - Progressive Scan Board I2C AD7196 bus busy

141222 - Progressive Scan Board I2C AD7196 read access time-out

141223 - Progressive Scan Board I2C AD7196 no read acknowledgement

141224 - Progressive Scan Board I2C AD7196 read failed

141225 - Progressive Scan Board I2C AD7196 write access time-out

141226 - Progressive Scan Board I2C AD7196 no write acknowledgement

141227 - Progressive Scan Board I2C AD7196 write failed

141228 - Progressive Scan Board I2C AD7196 failed

141301 - Progressive Scan Route Enable failed

141302 - Generating test image in Host decoder failed

141401 - Progressive Scan Route Disable failed

141402 - Turning off test image in Host decoder failed

141501 - Progressive Scan Board I2C failed

141601 - Progressive Scan Board I2C failed

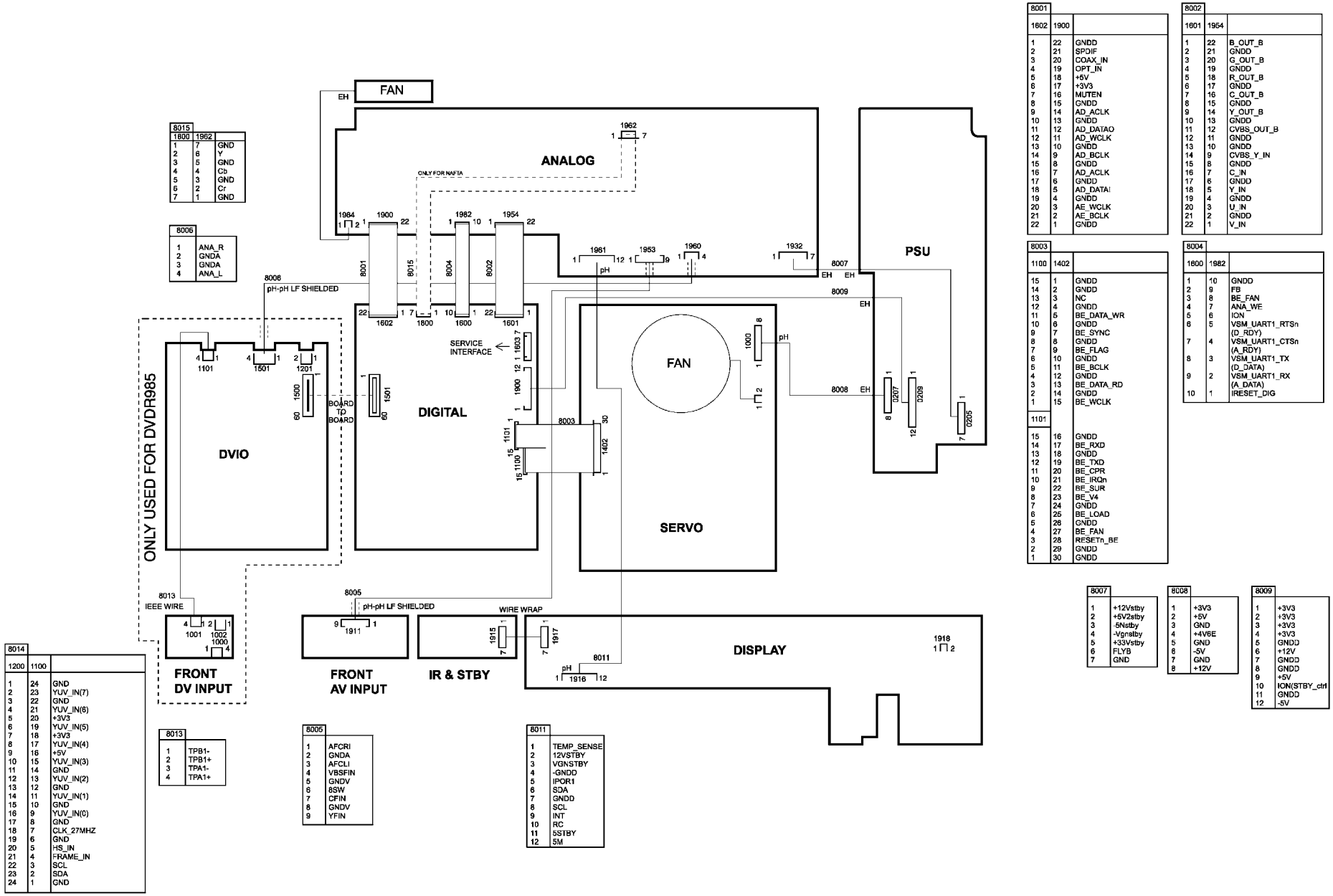


Figure 14 – Board Interconnect

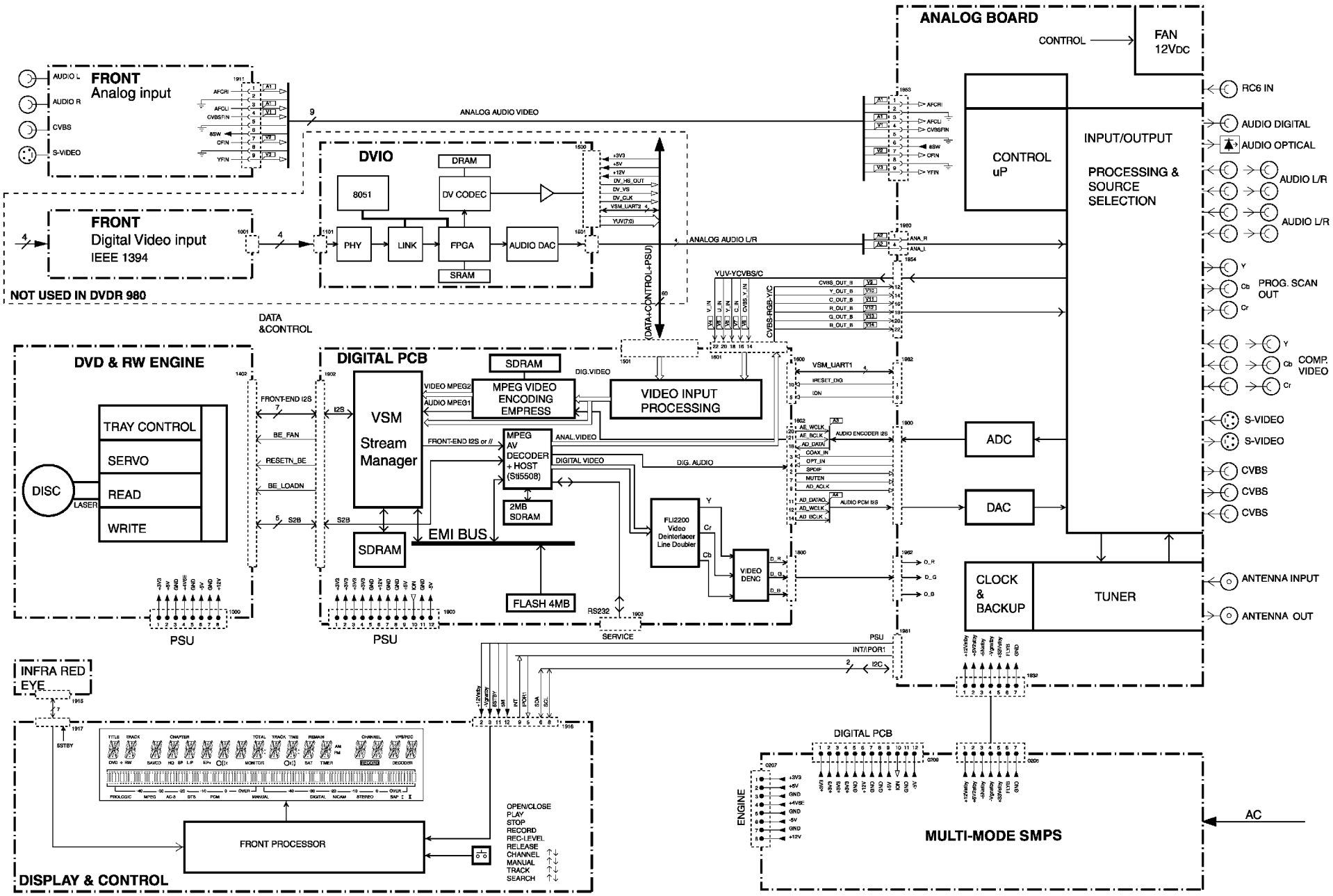


Figure 15 - Overall Block

Overall Block

Key Components

The unit is made up of: the Power Supply, the Front Panel, the Basic Engine, the Digital Board, the Analog Board, and the Digital Input/Output Board. Refer to **Figure 15.**

Block Diagram Descriptions

Power Supply
The Power Supply is a SMPS using Hot Ground on the primary side of the transformer. There is no MAINS power switch. It is operating when AC is applied. It supplies power to: the Analog Board, the Digital Board, and the Basic Engine.

Front Panel Display
This module contains a microcomputer that doubles as a fluorescent display driver. It receives the IR inputs and the keyboard inputs. It communicates the user input from the Keyboard and IR Receiver via the I^2C Bus to the Microcomputer on the Analog Board.

Basic Engine (BE)
This consists of the Mechanism and Servo control PCB. The Mechanism is essentially the same as a DVD with the exception of the Optical Pickup Unit, OPU. The OPU has a duel direction signal path, one for the write signal and one for the play signal. The OPU has three ICs mounted on it for processing laser signals. These include: the Laser Drive IC or LADIC, the Dvd Recordable Optical Preprocessor IC or DROPPI, and the Non Volital RAM or NVRAM to store its electro-mechanical settings.

The Servo controls the Mechanism. It handles the HF signal to and from the OPU. It uses a Microcomputer to control all aspects of the Servo operation. This includes: tray operation, spindle speed, focus, HF preprocessing, and radial positioning of the Light Pen.

Digital PCB

This module performs many functions. It interfaces between the Basic Engine and the rest of the unit.

During record, it encodes analog video into a recordable digital data stream. The Analog to Digital Converter is in a Video Input Processor, VIP, that supplies the MPEG2 Encoder. The Empress is the MPEG2 encoder. It supplies the data to the VSM, Versatile Stream Manager. The VSM is the gateway to the BE.

During playback, the MPEG2 Decoder receives its input directly from the BE. It decodes the data stream into analog Video. The analog Video is sent to the Analog Board and Digital Video is provided to the Line Doubler. The Line Doubler receives 11 bit digital YUV. The Line Doubler produces progressive scan digital Y, Cr, Cb that goes to the Digital to Analog Encoder. D_R, D_G, and D_B are sent to the Analog Board. The MPEG2 Decoder sends Digital Audio to the Analog Board to be processed.

Analog PCB
This module contains all the A/V inputs and outputs including a Tuner. There is no RF modulator. The RF output to the TV is merely a Loop-thru for the Antenna or Cable signals. Source selection and output type are controlled by a microcomputer. The microcomputer controls many functions throughout the unit including: user input, input/output selection, the Tuner, the DAC, and ADC functions of the Audio. It also controls the Fans.

DIVIO PCB
The Digital Input Module provides IEEE 1394 translation to the DVD recorder. It separates the Digital Video and Audio. The Digital Audio is decoded and sent as Analog Audio to the Analog Board. Digital Video (DV) is supplied to the Video Input Processor on the Digital Board.

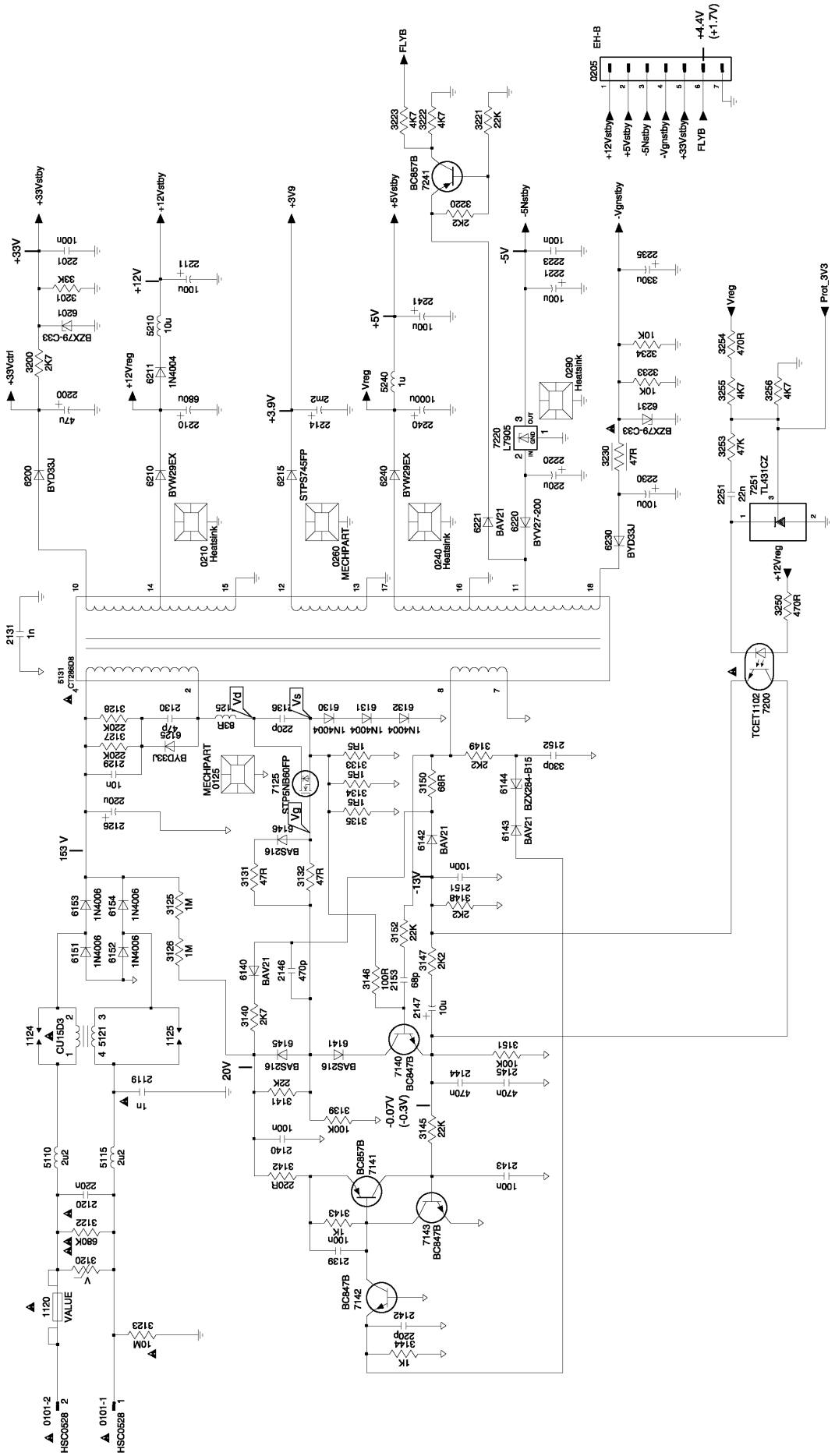


Figure 16 - Power Supply Circuit

Power Supply

This unit uses a stand alone Switch Mode Power Supply, SMPS. A MOSFET transistor turns On and Off in an oscillator fashion, driving a transformer. The primary half of the supply uses a Hot Ground. The primary side of the circuit provides drive and coarse control of the power supply. The secondary side of the circuit rectifies and filters the output of the transformer to produce many output voltages. It uses a cold ground, signal ground system. Two of the output voltages are monitored for precise regulation. The 12Vdc is supplied to the anode of the Optic Coupler's diode, and the 5Vdc Standby is feed to the Shunt Regulator. The regulation path includes an Optic Coupler to accommodate the different grounding systems.

Circuit Description

AC Input Circuit
Refer to **Figure 16**. The input circuit consists of a lightning protection circuit and an EMI filter. The lightning protection circuit consists of R3120, spark gaps 1124 and 1125. L5110, L5115, C2120 and L5121 form the EMI filter. It prevents noise coming in or out through the mains. The AC input is rectified by diodes 6151, 6152, 6153, 6154, and filtered by C2126. The voltage on C2126 is approximately 155V. It can vary from 150V to 160V, depending on the AC input voltage.

Start Circuit
This circuit consists of R3125, 3126, R3139, R3141, C2140, and R3132. When the power plug is connected to AC, the MOSFET 7125 will start conducting as soon as the gate voltage reaches the threshold value. A current starts to flow in the primary winding of 5125, Pins 2 and 4. The MOSFET will be fed forward via the winding connected to Pins 7 and 8 by R3150 and C2146. While the MOSFET is conducting, energy is building up in the transformer. The current flow through the MOSFET is sensed by R3133, 3134, and 3135. When the current level rises high enough to provide a voltage drop on these components and large enough to turn On 7140, 7125 is turned Off by 7140. Diodes 6130, 6131 and 6132 protect the control circuit in case of failure of the MOSFET by providing an upperlimit to the voltage that can remain on the source of the MOSFET.

Coarse Regulation
The positive portion of the signal on Pins 7 and 8 will be rectified via R3150 and D6140, charging C2140 via R3140. In time, the voltage on C2140 will reach 15 to 20Vdc. This value depends on the value of the Mains voltage and the load. The negative portion of the signal on Pins 7 and 8 will be rectified via R3150 and D6142. This will charge C2151 to approximately -15Vdc. This is used as a regulation supply.

The control circuit consists of T7140, D6141, C2144, C2145, C2147, R3147, and 3148. This circuit controls the conduction time and the switching frequency of the MOSFET. It switches Off the MOSFET as soon as the voltage on the source of T7125 reaches a certain value. This value depends on the error voltage at the emitter of T7140, which can be a negative (+/- 0.6V). The voltage fed back by the regulation circuit defines this error voltage.

Precise Regulation
The regulation circuit consists of an Optic-Coupler, 7200, 7251, and a voltage divider network. The Optic-Coupler isolates the Hot Ground referenced voltage on the emitter of 7140 from the Cold Ground referenced voltage on 7251. 7251, a Shunt Regulator, has two component characteristics. It is a very stable and accurate reference diode and a high gain amplifier.

7251 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5Vdc. If the reference voltage is lower, the cathode current is almost zero. The cathode current flows through the LED of the Optic-Coupler, controlling the current through the transistor portion of the Optic-Coupler. The collector current of 7200 will adjust the feedback level of the error voltage at the emitter of T7140.

Overcurrent Protection Circuit
This circuit consists of R3145, C2143, a thyristor circuit formed by T7141 and T7143, R3143 and R3142. When the output is shortened, the current through the FET will produce a large voltage drop across the source resistors of the FET. That voltage turns On 7140 and 7143. The thyristor circuit will start to conduct and switch Off the supply voltage to C2140. This switches Off the drain current of the MOSFET, 7125. The start circuit will try to start up the power supply again. If the short still exists, the complete start and stop sequence will repeat. The power supply is in a hiccup mode and is ticking.

Overvoltage Protection Circuit
This circuit consists of R3149, D6144, 6143, R3144, C2142 and T7142. If the regulation circuit does not function due to an error in the control loop, the regulated output voltage will increase. This overvoltage is sensed on the hot ground side of the transformer at Pins 7 and 8. When an overvoltage is detected, the circuit will activate the thyristor circuit T7141 and 7142. The power supply will be shutdown as long as the error in the control loop is present.

Secondary Rectifier/Smoothing Circuit
There are six Rectifier/Smoothing circuits on the secondary side. Each supply voltage depends on the number of windings in the transformer. From these circuits, several voltages are derived and fed to three connectors. The following voltages are present at the output: 33Vdc, 12Vdc, 3.9Vdc, and 5Vdc Stby, -5Vdc Stby, and -33Vdc Vgnstby. The +12V is switched Off by the STBY_Ctrl signal, ION. The -33Vdc is dedicated to the Front Panel Fluorescent Tube as a grid supply. The FLYB signal is used as a Power Fail and measurement signal.

Front Panel

The main elements of the Front Panel are the microcomputer, 7156, the Display Tube, and the keyboard. Refer to **Figure 18**. 7156 is an 8 bit microcomputer fitted with 96kB ROM and 3kB RAM and is responsible for the following functions:

Fluorescent Display driver

Monitoring the keyboard matrix

Decoding the remote control commands from the infrared receiver, 6170.

Activation of the display

The Fluorescent Tube operates using a grid and segment scanning matrix. AC is supplied by a switching regulator consisting of 7151, 7152, 7153, and 5153. With AC supplied, the microcomputer scans the elements in the tube to determine what segments light up. The system clock is generated with the 12MHz crystal, 1153.

Keyboard Matrix
There are 11 different keys on the display board. A resistor network is used to generate a specific voltage value, depending on the key pressed, via the resistors 3186-90, 3145, 3197, 3177-3178, 3197, and 3180. This RTL data (voltage Level) is sent to 7156 on Pins 17, 18, 19, and 20. Pressing keys simultaneously may lead to undesired functions!

Button	*A/D input (v)*
Record	4,776
Stop	4,098
Play	3,405
CH +	2,5
Man +	1,562
Track -	0,088
Search -	0,454
Rec Level	4,098
Release	3,405
CH -	2,5
Man -	1,562
Track +	0,088
Search +	0,454
Stand By	4,776
Open/Close	0

Figure 17 - RTL Voltage Chart

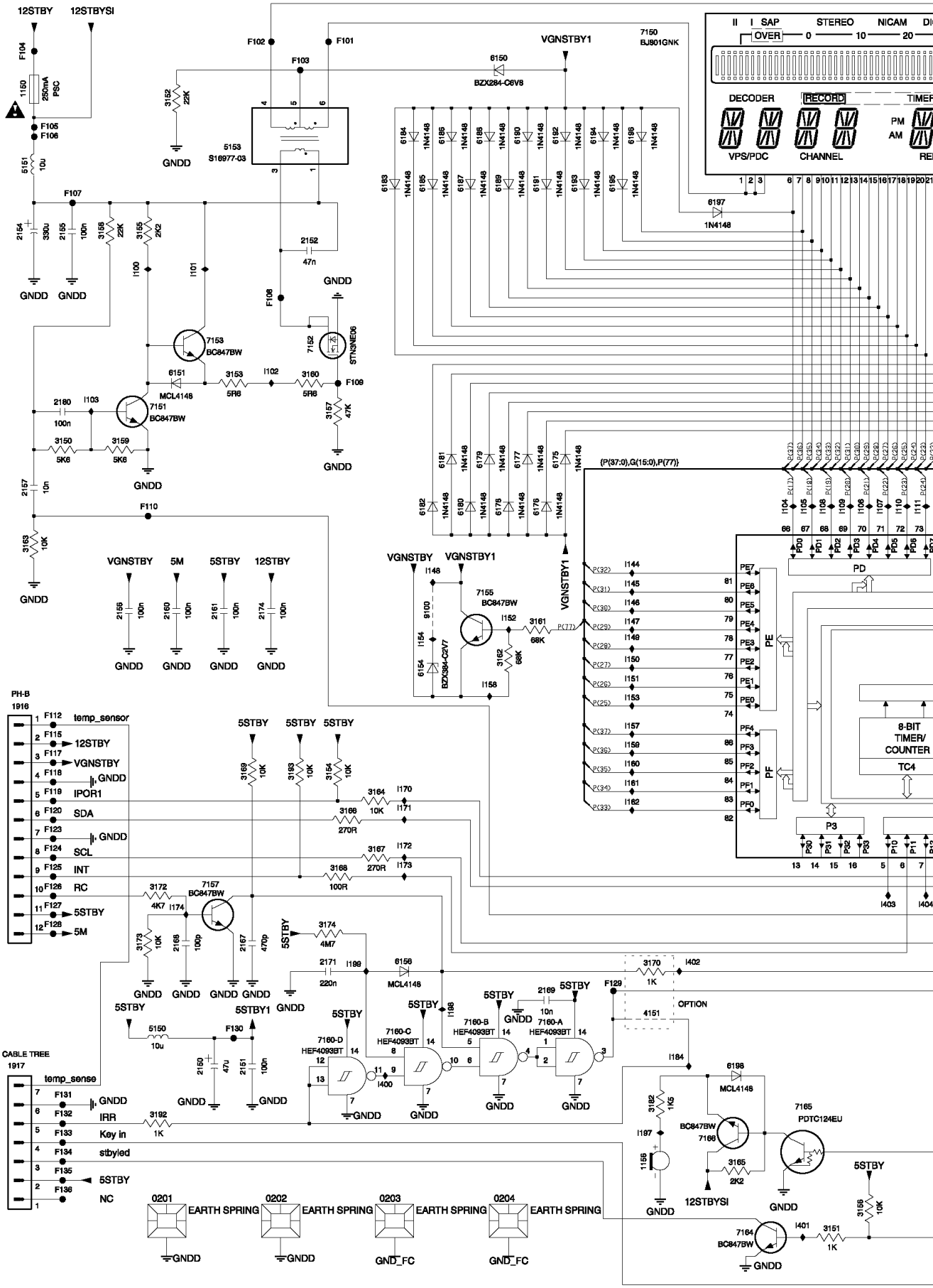
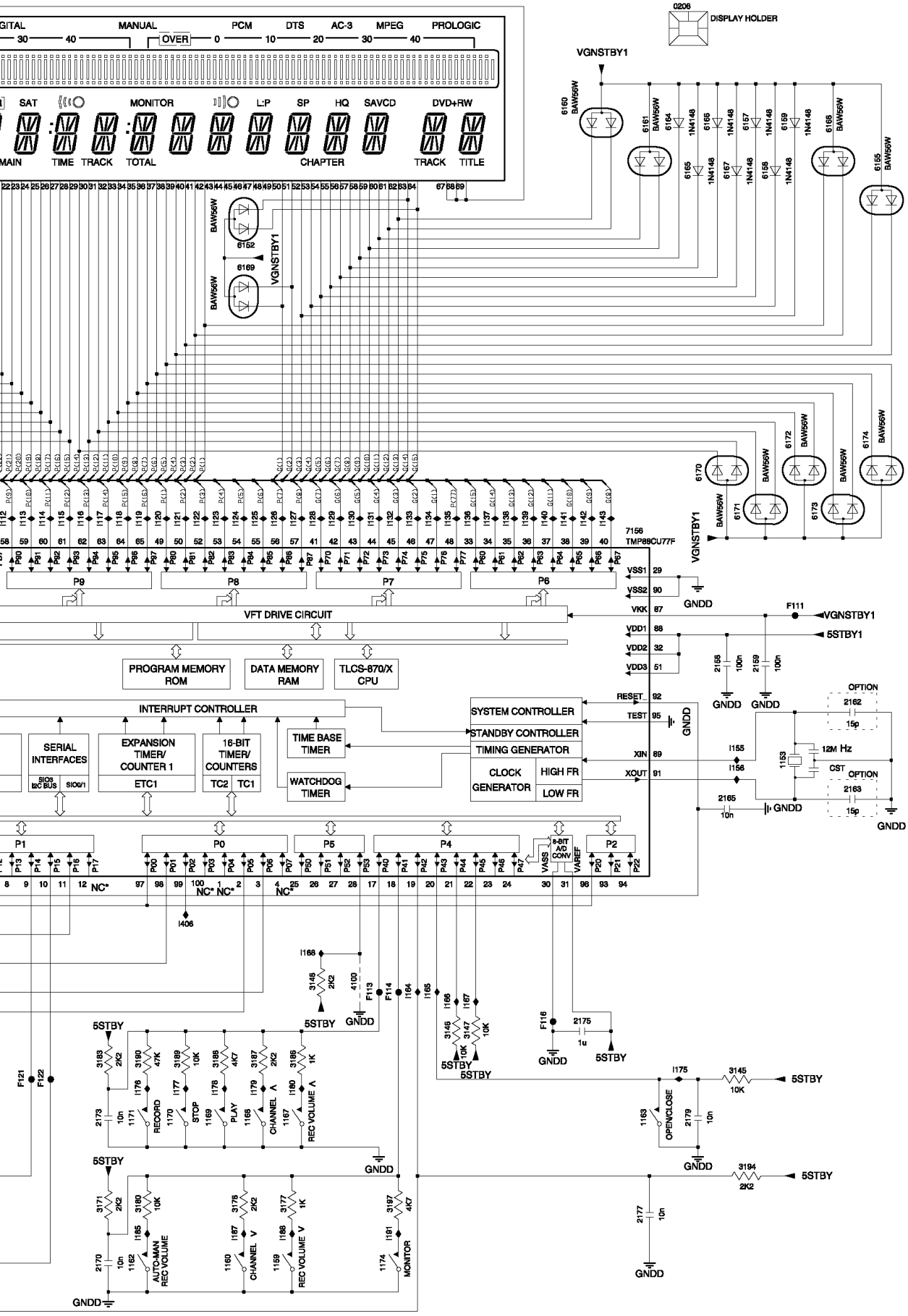


Figure 18 - Front



Panel Circuit

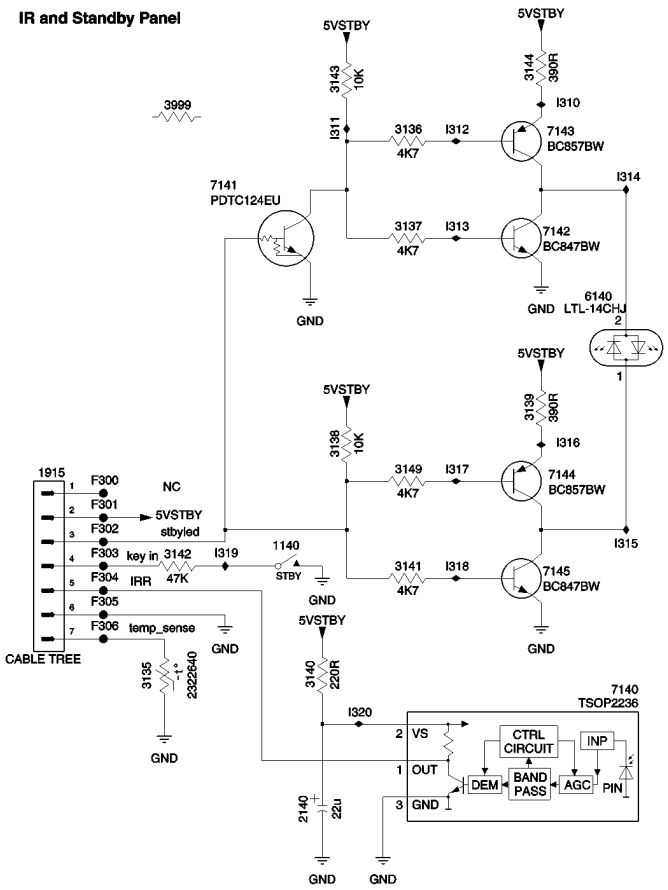


Figure 19 – IR and Standby Panel

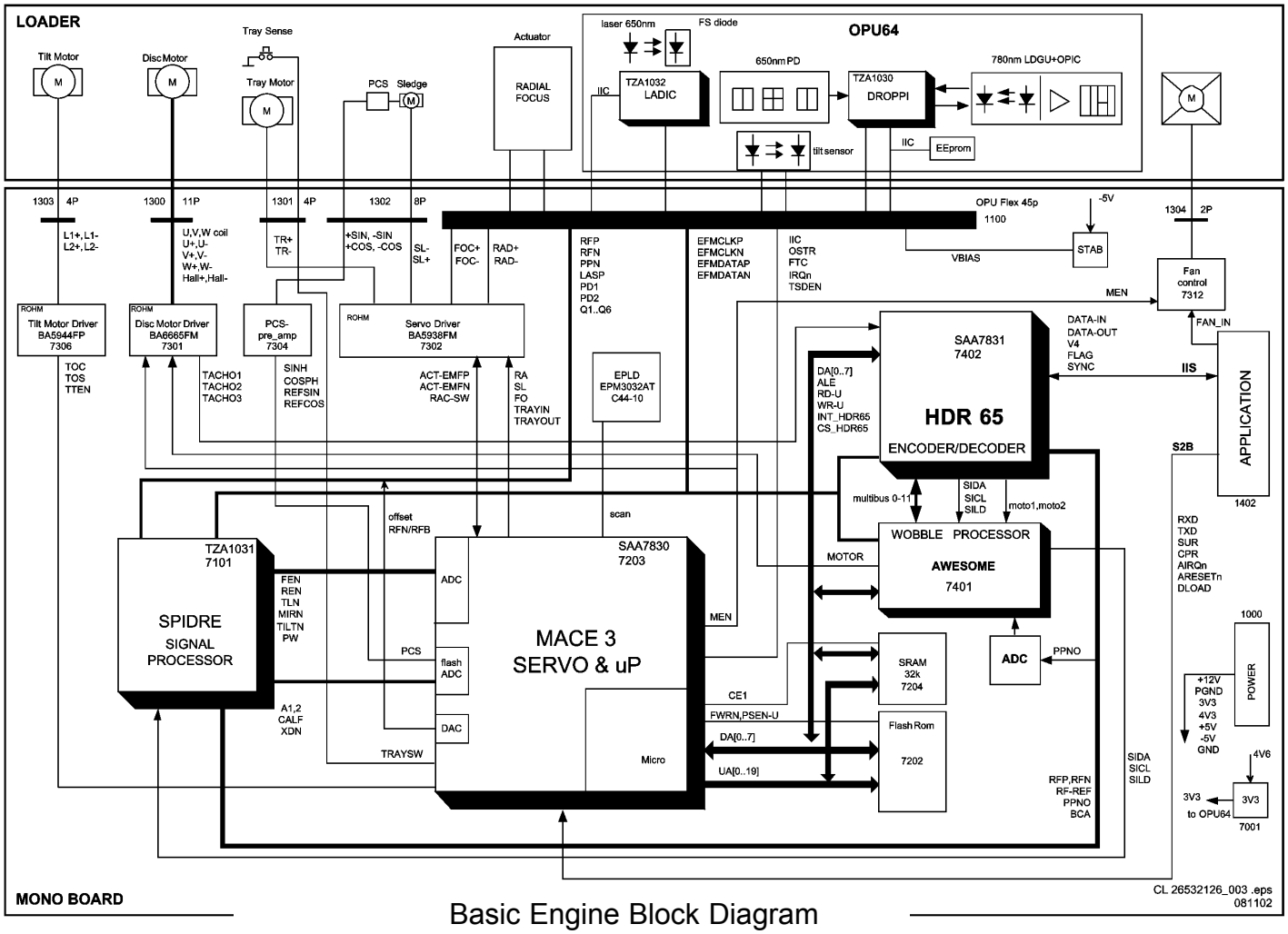
IR Receiver

The IR receiver, 7140, contains a bandpass amplifier as well as a photo-diode. Refer to **Figure 19**. The photo-diode receives approximately 940nm infrared pulses. The pulses are amplified and demodulated. On the output of the IR receiver, 7140, is a pulse sequence at TTL levels. The IR signal appears on Pin 5 of 1917 on the Front Panel. The IR signal goes to Pins 12 and 13 of 7160. 7160 establishes a minimum threshold for the IR signal to trigger its gate. This filters out erroneous IR from reaching the Microcomputer.

The RC connection on the rear of the unit comes through the Analog PCB to 1916 Pin 10. This signal also goes to 7160, Pin 5. This pulse sequence is an input to the controller for further signal evaluation via IRR input on 7156, pin 2.

Bi-Color LED (Standby and ON)
The STBY-LED is a red/green bi-color-LED controlled by the STBYLED signal on Pin 10 of 7156. The LED drive circuit receives the 5Vdc Standby supply. The control voltage coming from the Microcomputer is inverted by 7164. When the LED control voltage on the microcomputer is High, a Low goes to the LED drive circuit, turning the LED green.

Figure 20 - Basic Engine (BE)



Basic Engine Block Diagram

DVD Mechanism and Servo Board

Basic Engine

The Basic Engine consists of a DVD-Mechanism with dual laser Optical Pickup Unit (OPU), a tray loader, a fan unit, and a PCB containing all electronics to control the module. The OPU contains the Focus and Radial Motors. The Mechanism holding the OPU contains the Sled and the Tilt Motors. The electronics of the module are responsible for all the basic servo tasks. It reads and writes data to and from the disc.

The PCB is multilayer, using Surface Mounted Circuitry with a very high component density. Detailed diagnostics and fault finding are available via ComPair.

Some specifications:

* Record DVD+R and R/W
* Lossless linking
* Recording speed: 1.2 x
* Playback DVD, DVD+R(W), DVD (SL/DL), DVD-R, DVD-RW (V1.1)
* Playback speed: 1.2 x
* Playback CD, CD-DA, CD-R, CD-RW, CD-ROM, VCD/SVCD
* Playback speed: 3 x
* It controls all other functions like tray control, start/stop, disc rotation, tracking, jumping, and communication to the Digital Board.

The Servo circuit provides the interface between the Mechanism and The Digital Signal Processing Board. It is mostly on one board attached to the bottom of the mechanism. It is made up of four main circuits:

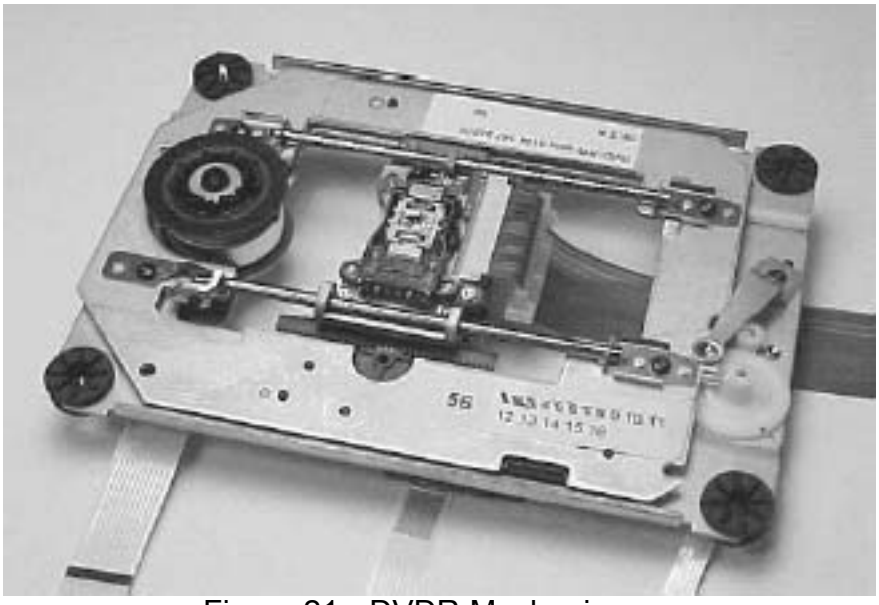


Figure 21 - DVDR Mechanism

* The SPIDRE is the Signal Processor IC for DVD Recordable
* The MACE3 is the Mini All in one CD Engine third generation.
* The Encoder/Decoder is the Translation circuit for data going to and from the disc.
* The AWSOME is the Adip Decoding, Wobble Proccesing, Error Correction, Synchronous start Stop and Occasionally Mend Errors

Initialization process
During power-up, a reset of the BE is preformed. This is parallel to the reset process of the Digital Board. After the MACE3 resets, a System reset occurs to reset the other microcomputers in the BE. A self-test will automatically start. Each of the microcomputers must respond to the I^2C bus. The SDRAM and flash are also tested. If the self test passes the SUR signal line will go Low. Part of the self test is the CPR switching voltage coming from the Versital Stream Manager. If it is ready to function, it will be Low. After the self test passes, the BE will wait for the first Serial to Basic Engine, S2B, user command. E.g. "Tray_out".

Disc recognition process
The process of disc recognition is entirely performed within the BE. If the disc is not recognized, the problem is in the BE or something missing supplied to the BE. Information about the disc type is sent via the Subcode data path to the MPEG2 Decoder microcomputer.

DVDR Mechanism

The DVDR-M is made up of three components: Optical Pickup Unit, OPU, the Sled, and the Turntable Motor. The OPU contains two lasers: one for CDs with a wavelength of 780 nm, and one for DVDs with a wavelength of 650 nm.

The OPU contains: the Optics, the Focus Motor, the Laser Drive IC (LADIC), the Tilt sensor, the DVD Rewritable OPU Pre-Processor IC (DROP-PI), and the EEPROM with the OPU adjustment data.

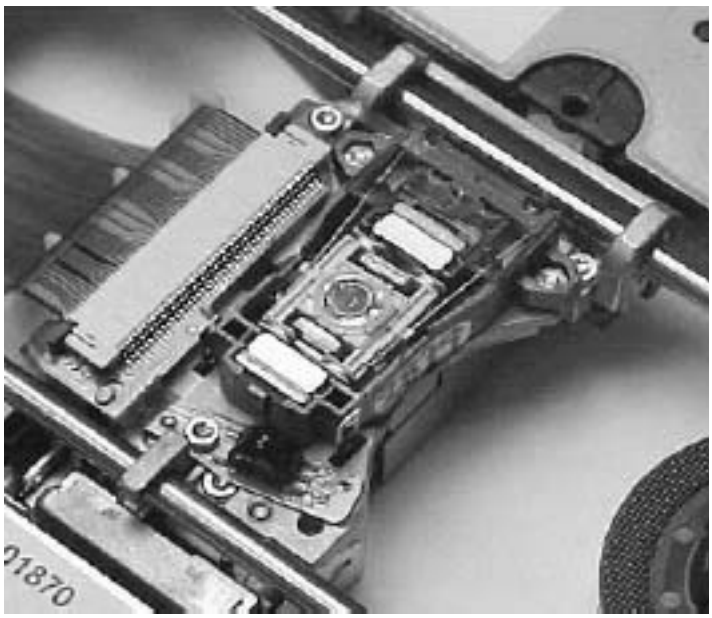


Figure 22 - Optical Pickup Unit

DROPPI

The DROPPI (DVD Rewritable OPU Pre-Processor IC) is a multi-purpose analog pre-processor. It supports many photo detector configurations and output signal modes. It produces RF and servo feedback signals, Q1-Q6. Its output signals are on the same flex ribbon cable with the wideband RF (differential signals). The Wobble, focus, and Sled Servo signals are relatively low bandwidth.

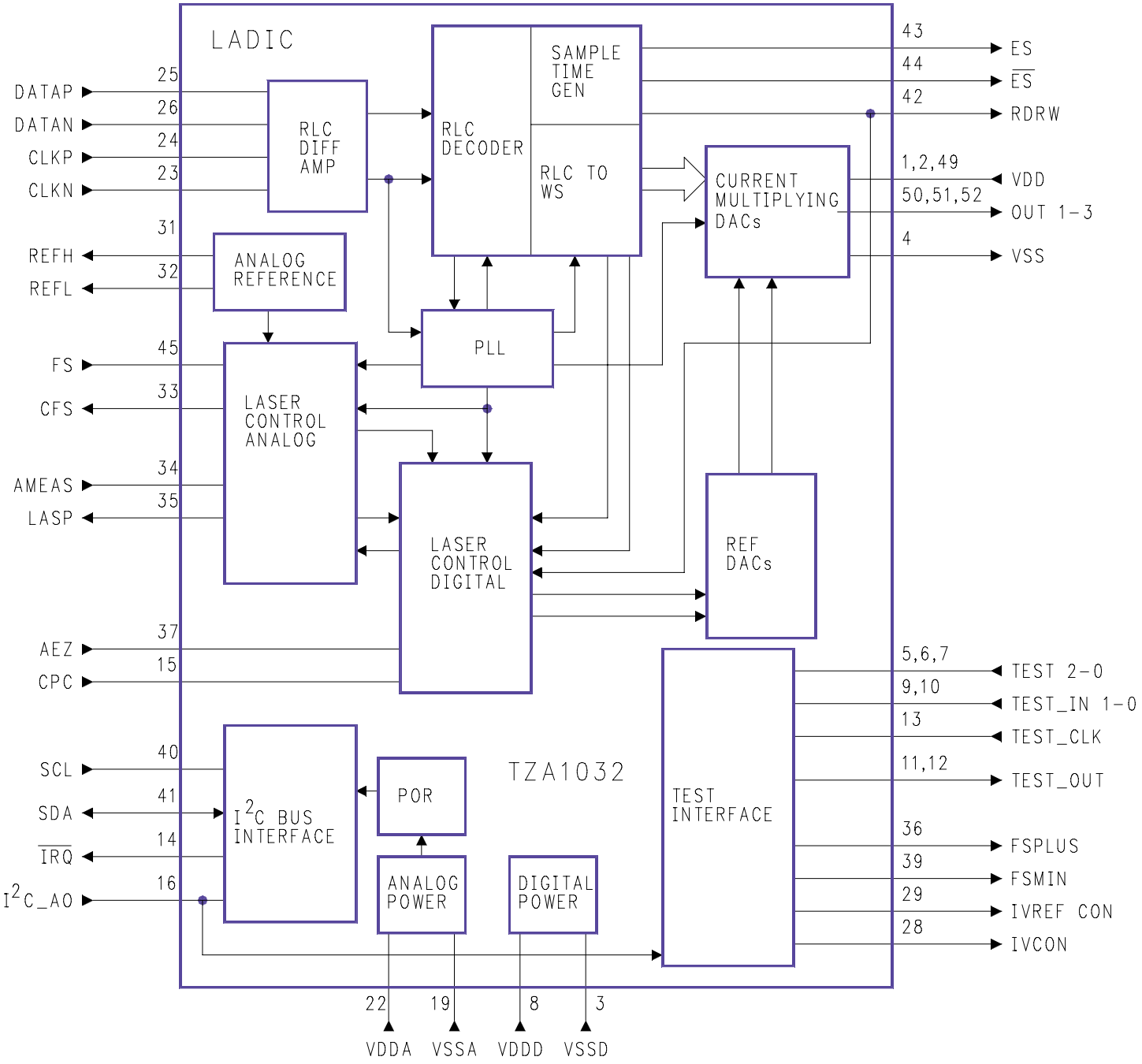


Figure 23 - Laser Drive IC

LADIC

The Laser Drive IC, LADIC, controls the data to the lasers, and the supply to them. It performs three main functions:

- It drives the laser for both playback and record functions. Its greatest stress is realized during record, producing data signals and write pulses. The recording process is flexible with respect to the input modulation method (EFM, EFM+, 17 pp, etc.). This is necessary to support CDR/RW and DVDR/RW. To accomplish this, the LADIC uses two Random Access Memories (RAM) which can be loaded (non real-time) via the I^2C Bus from the microcontroller.

- It drives the laser with a sequence of programmable write pulses with high timing accuracy and high peak current levels.

- It controls the exact light power levels coming from the laser and controls the exact power absorbed by the disc during recording.

The LADIC needs three independent power supplies. These are the analog and digital power supplies, and V Bias for the laser driver function. The supplies are separate to obtain maximum output performance where there are large and highly dynamic current flows.

The LADIC is controlled by an I^2C bus. The laser is operated at three current levels: Playback, Record and Erase. During the initilazation of a disc to be recorded on, and test recording is preformed in a special place on the the inner most section of the disc. A series of random data is recorded with a wide range of current levels. The data is played back. Two feedback signals are generated and sent to the MACE3 circuit, A1 and A2. A second Fine tuning of the Optimal Laser Current is preformed. The disc is written to again except the current range is chosen by the MACE3 using the feedback received. This fine tuning of the laser current produces the Calf feedback signal that is sent to the MACE3 and it is stored in the MACE3's operating RAM.

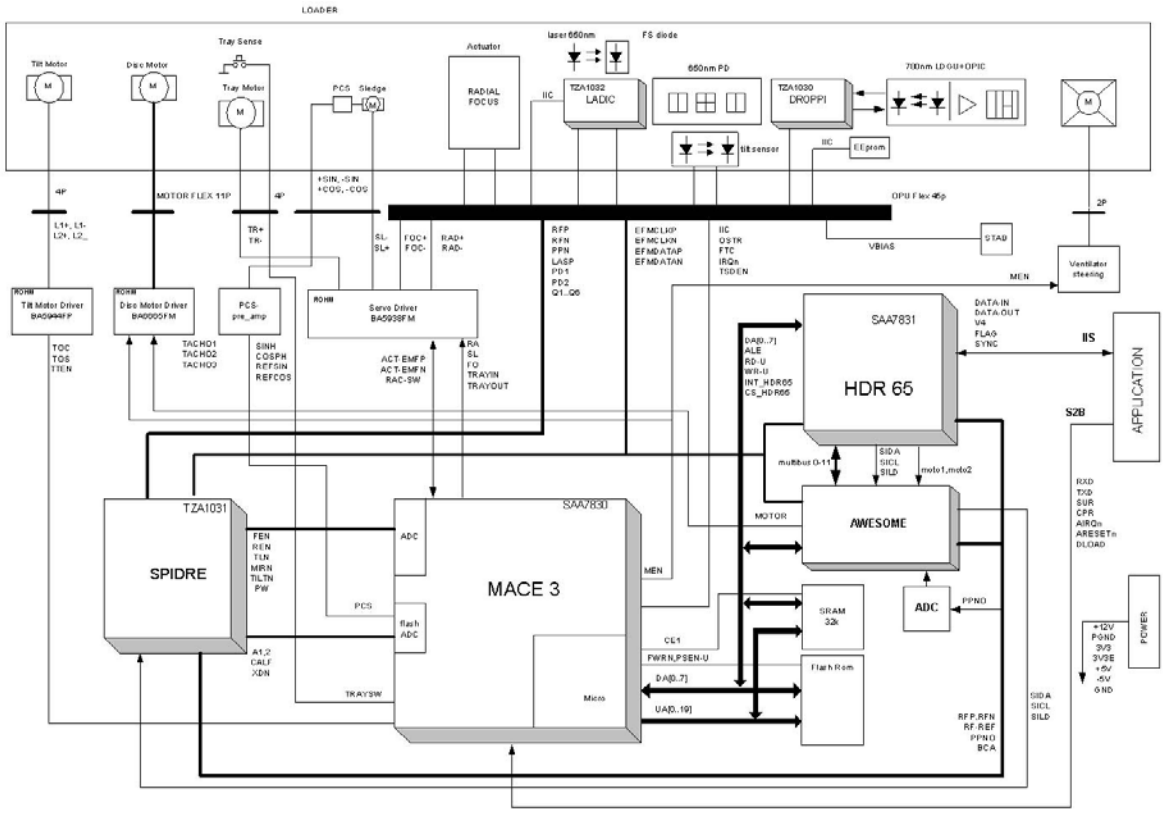


Figure 24 - Servo Block Diagram

BLOCK DI

Servo Circuit Description

The Servo circuit provides the interface between the Mechanism and The Digital Signal Processing Board. It is mostly on one board attached to the bottom of the mechanism. It is made up of four main circuits:

The SPIDRE
The MACE3
The Encoder/Decoder
The AWSOME.

Servo Power and Reset
The Servo receives: 12Vdc, 5Vdc, 3.3Vdc and -5Vdc from the Power Supply. There are three 2.5V supplies on the Servo Board connected to the 3.3Vdc supply. The MACE3 is reset by the Digital Board, via the Reset_BE signal. A Reset signal comes from the MACE 3 for the rest of the servo. The Mace3 is the Host for the local I^2C Bus.

SPIDRE

The SPIDRE (Signal Processing IC for DVD REwritable) is a multi-purpose analog pre-processor IC specifically intended for writing applications.

The SPIDRE receives two Power Supplies: -5Vdc and 5Vdc. Its has three main tasks. One is is to interface the Servo signals that go to the MACE3 Servo Processor. The Second is Preprocessor for the RF signal coming from the disc during playback. The third is to process the RF signal coming from the Encoder during record.

The SPIDRE is controlled by the AWSOME via a serial bus on Pins 35, 37, and 38. The AWSOME communicates: gain information, data type, and operation mode, Play or record.

The Servo signals to be processed include: Playback HF/RF, the focus servo feedback signals, the radial feedback, the track loss signal,

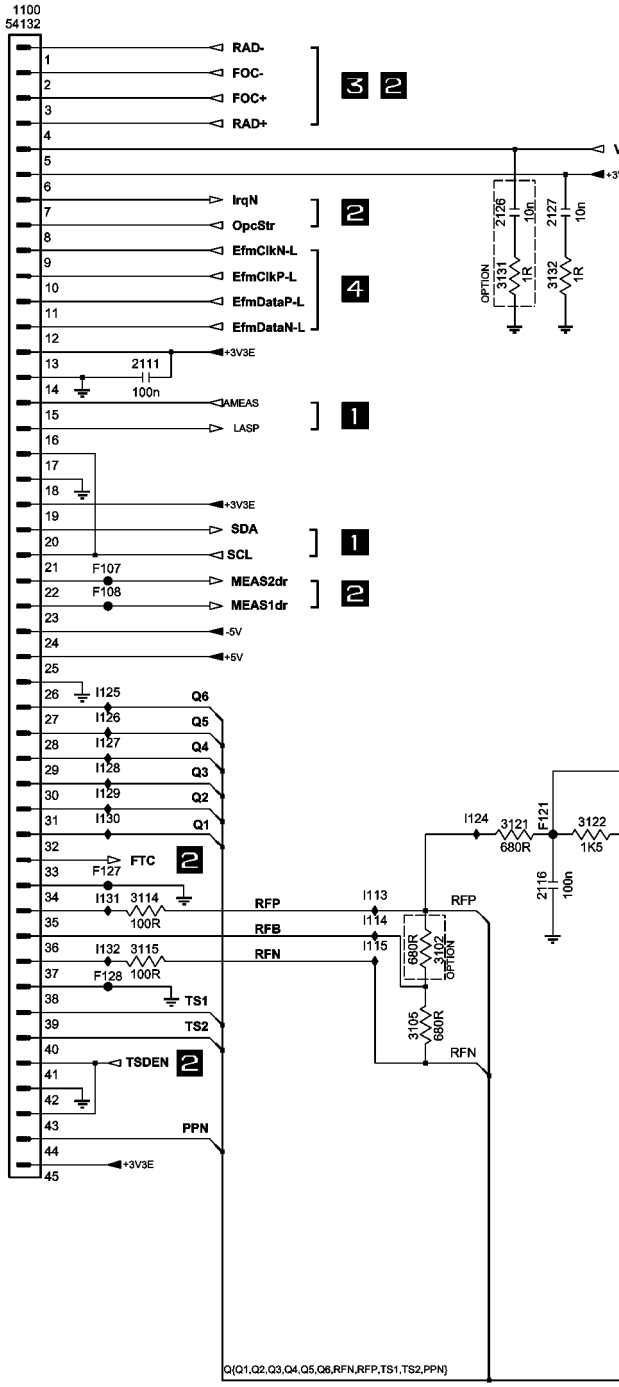
and tilt sensor signal. The HF/RF (EMF) signal varies greatly between disc formats. The Focus Error and Radial Error signals come from the mechanism on the Q1-6 signal paths. The Tilt Error has a Photo Tilt Sensor. The dynamic range of these signals is very large. They are converted to Lower frequency RF data paths that the MACE3 can accommodate. This is required for playability of the many different kinds of discs.The error signals are all balanced to reduce noise interference. Thus, they are named XX positive, and XX negative. The Output signals include: the Focus Error, the Radial Error, the Tilt error, laser PoWer, and tracking loss signals.

The Record RF EFM data and EFM Clock comes from IC 7402, Encoder circuit, and is supplied to the SPIDRE on Pins 48-51 of 7101. The SPIDRE processes the RF signals for gain control of the Error control signals going to the MACE3 during record. All of these signals are balanced. Thus there is a negative and a positive signal for all of them.

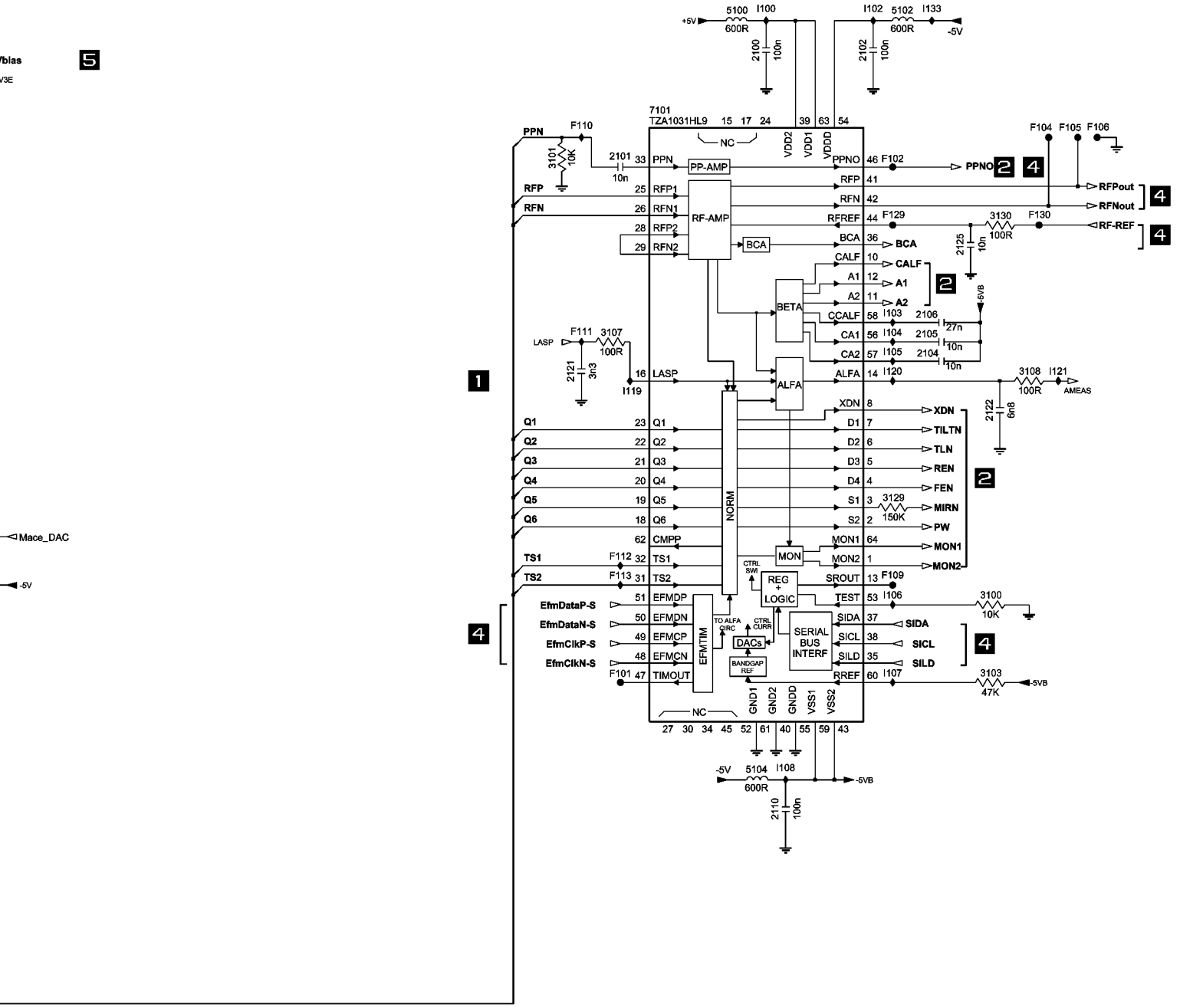
The LASP, Laser Power feedback signal is processed by the SPIDRE. During playback, the EFM coming from the disc is used by the ALFA circuit to generate the AMEAS, ALFA Measurement, signal that goes back to the LADIC for precise control of the LASER power. During record the EFM signal coming from the Encoder is used by the ALFA circuit to create the AMEAS signal.

The pregrove tracking error signal comes from a Preprocessor in the OPU. The PPN signal is amplified and sent to the Wobble Processor in the Decoder circuit.

1 PRE-PROCESSOR



Fi



CL 2

igure 25 - PRE- Processor

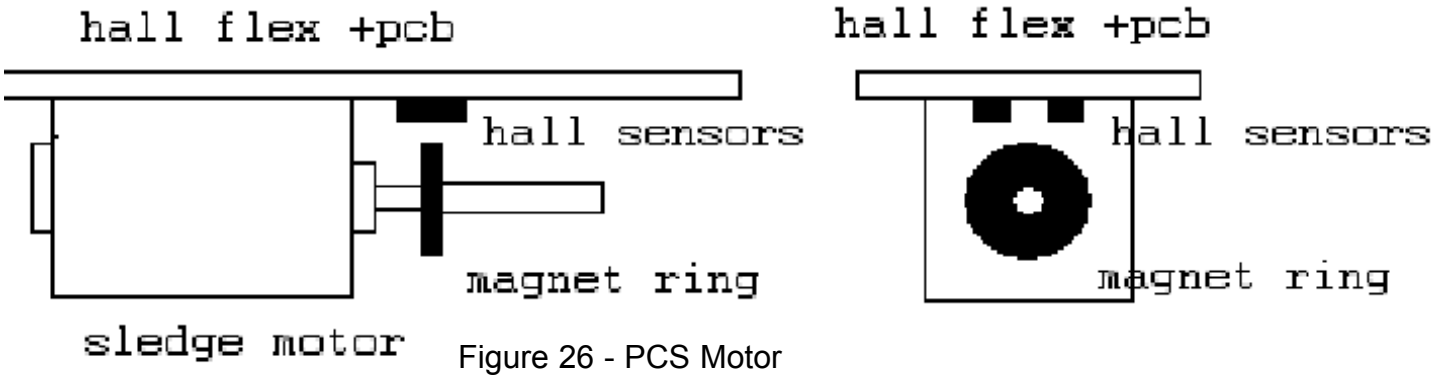


Figure 26 - PCS Motor

MACE3 Servo Microcomputer

The MACE3 IC is the Mini All Cd Engine third generation. Its vendor number is SAA7830. It is a combined servo processor and microcomputer. The servo processor handles the signals for focusing and tracking for disc access. It also generates the control signals for tray control. In a CD/DVD system, there are several active control loops. Some of them are needed to adjust the servo error signals. It monitors and adjusts the offsets, signal amplitudes, and loop gains (AGCs). The control loops determine the laser spot position on the disc in the radial (Sled),

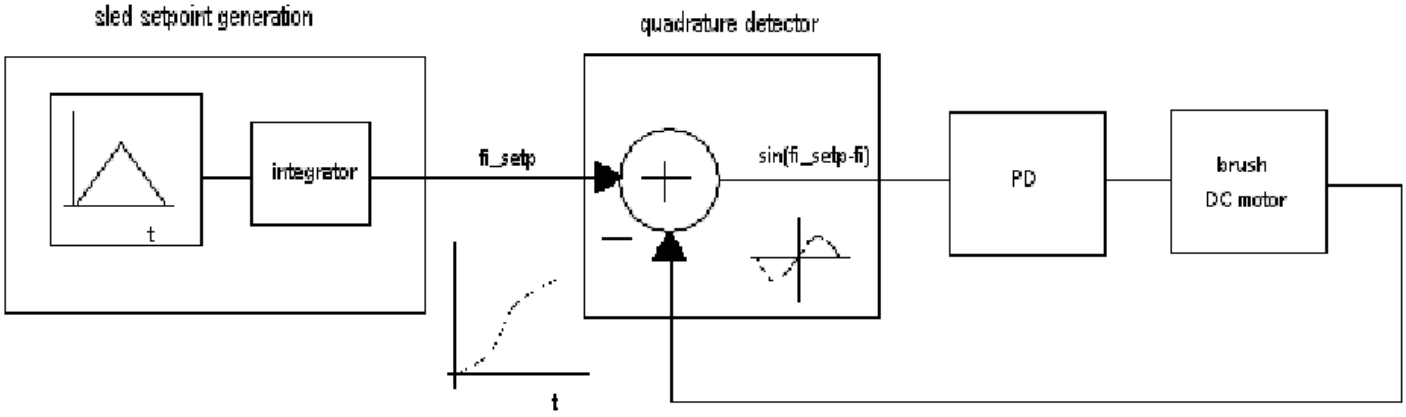


Figure 27 - PCS Phase compaision

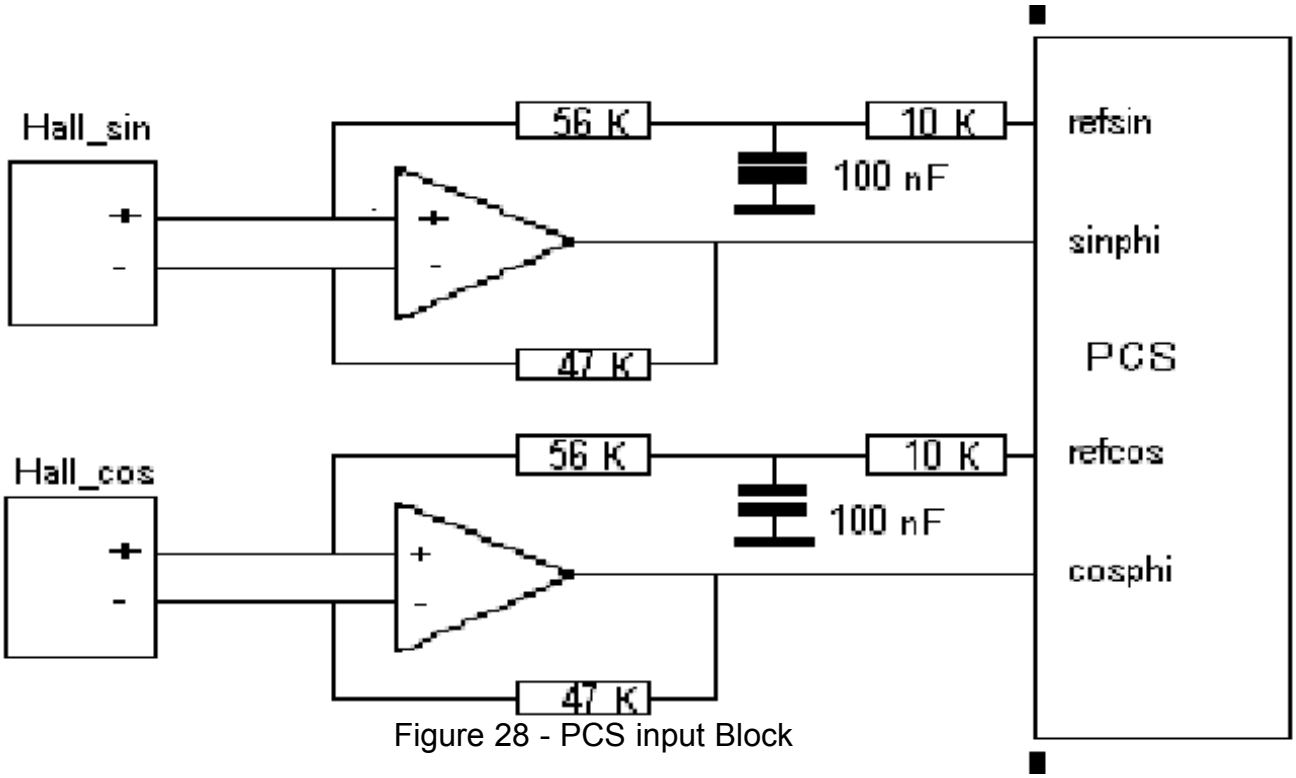


Figure 28 - PCS input Block

axial (focus), and tangential directions (Tilt). This access system consists of two parts, namely the Focus Actuator and the Sled, which are, within a certain range, mechanically and electrically independent.

The analog signals from the SPIDRE are converted into a digital representation using A/D converters. The digital codes are then applied to logic circuitry to obtain the various control signals.

OPC (Optimum Power Calibration)
This device has an integrated Optimum Power Calculation block for use in CDR, CD-RW, and DVD+R applications. It reads three analog signals: A1, A2, and CALF. These represent Max, Min, and Average values of the EFM coming from the disc, respectively. It also takes the Power (PW) signal from the laser controller and then feeds an analog signal, ALPHA0, out to control the laser power. The conversion frequency is 88kHz per channel. Basically, the OPC procedure tries to find out the optimum laser power to be used on a specific disc. It consists of three phases:

1. WRITE - Random EFM data is written to the test area of the disc at increasing levels of laser power, controlled by ALPHA0.

2. READ - The data on A1, A2, and CALF is read back from the test area and stored in memory.

3. CALCULATION - the embedded microcomputer then calculates the setting of ALPHA0 where the least jitter is encountered. Some preprocessing is carried out by the OPC logic to reduce the processor's load. This sequence is performed twice - first a coarse calibration, followed by a fine-tuning.

The micro controller has many responsibilities. It processes the Serial to Basic Engine, S2B, commands from the Digital Board. It controls the various processes in the mechanism via I^2C.

The MACE3 uses a Parallel communication bus for access to its Flash ROM. Refer to **Figure 29**. The Flash Memory contains the firmware for the BE. The MACE3, the Encoder and AWSOME share a parallel bus with 32K of SRAM

When the power is applied to the unit the Digital Board sends a reset signal to the MACE3. The MACE 3 checks its SRAM, the reads its Flash Rom and sends a System Reset signal to the ICs on the Servo Board. When its memory tests are complete and they pass, a SUR control voltage goes low, indicating to the Digital Board that it is ready to receive commands. It then initializes its I Square C Bus and communicates to the DROPPI and LADIC on the Mechanism. The Tilt Motor is exercised and centered. The PSEN signal then appears.

The Microcomputer produces several outputs. Many of them are error signals. It produces: the Radial Error, the Focus Error, the Tilt Motor control, and the Position Control Sled (PCS) signals. Each of the motors has a driver circuit.

The Microcomputer controls the Tray motor drive circuit. The Tray switch goes directly to the MACE3.

The Microcomputer controls the PCS. The Position Control Sled must operate very accurately. It cannot track the Disc's tracks of 1.6 microns alone, but its precision is a must. There are two Hall sensors positioned 90 degrees apart in a circular fashion. A round magnet is attached to the armature of the drive motor. The positioning of the sensors gives them their name, Sin and Cosine. The motor is a basic universal type. The exact rotation of the armature is detected by the Hall Sensors. The phase of the Hall sensor signals are compared to a reference signal generated internally by the MACE3. The focus actuator moves the lens side to side for tracking the individual tracks. When the drive current to the actuator increases to a certain point, the microcomputer knows the Sled must be moved. The Sled is driven to minimize the actuator's drive current, meaning it is right under the proper track. The microcomputer produces the Reference DC offset for the Op amp inputs.

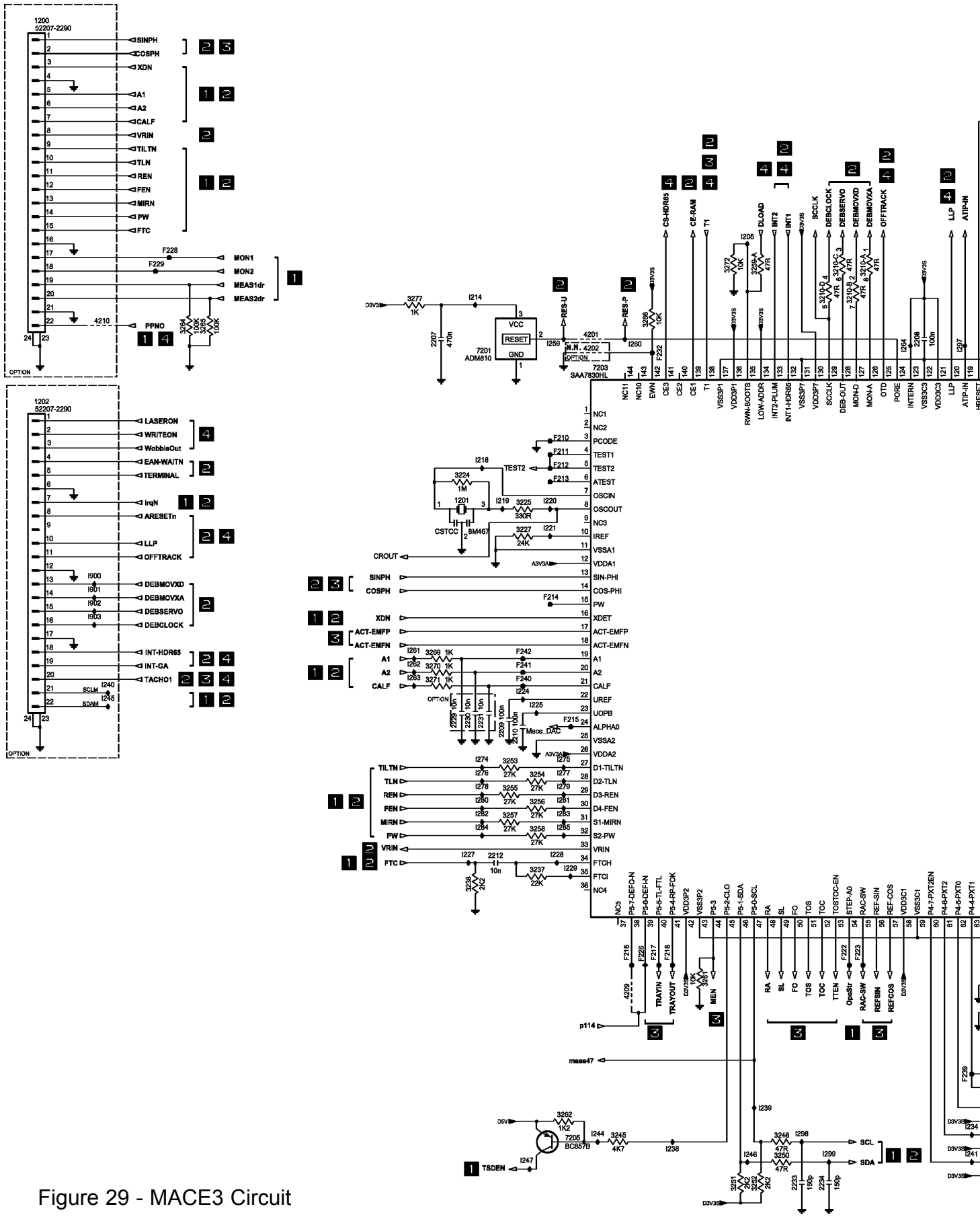
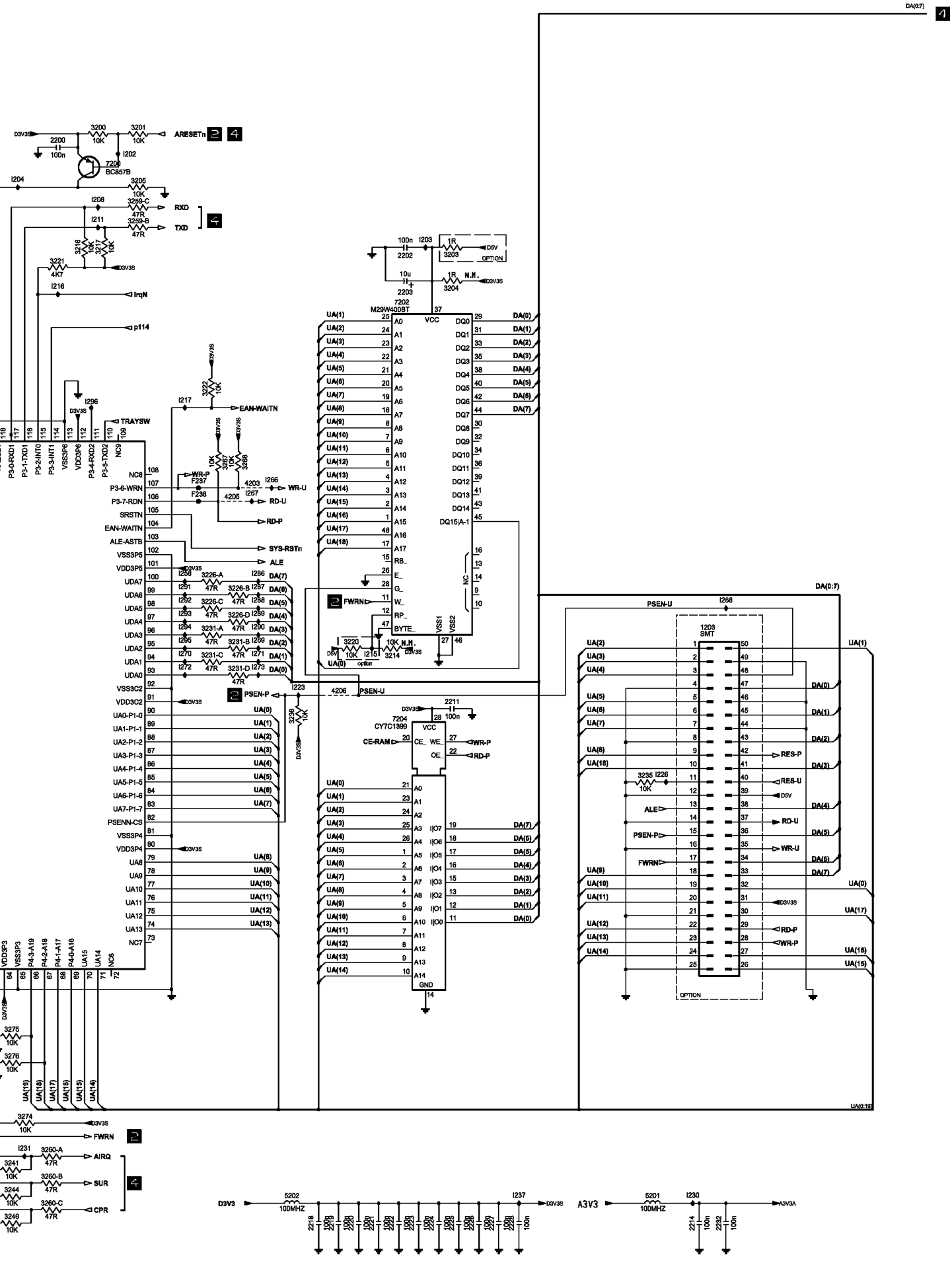


Figure 29 - MACE3 Circuit


DA(0:7)
ARESETn
RXD
TXD
IrqN
p114
TRAYSW
EAN-WAITN
WR-P
WR-U
RD-U
RD-P
SYS-RSTn
ALE
PSEN-P
PSEN-U
FWRN
7202
M29W400BT
7204
CY7C1399
CE-RAM
1203
SMT
OPTION
RES-P
RES-U
AIRQ
SUR
CPR
D3V3
A3V3
UA(0:19)

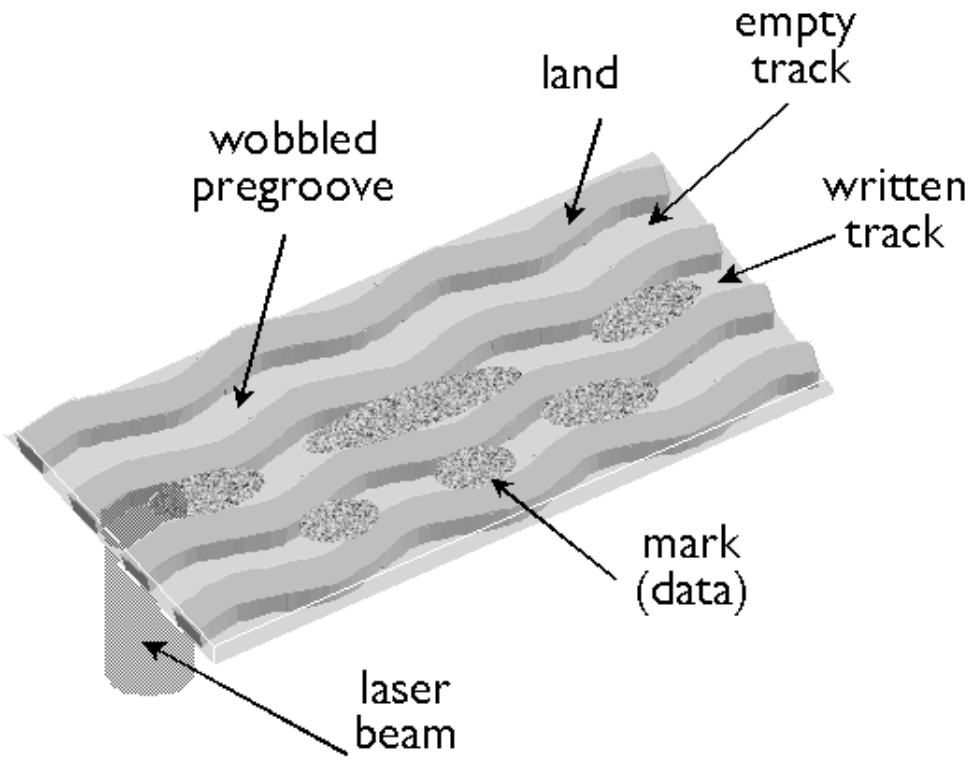


Figure 30 - Wobble Tracks

Wobble

A Pre-groove is stamped on writable discs. All recordable DVD media types feature a microscopic wobble groove embedded in the plastic substrate. This wobble provides the recorder with the timing information needed to place the data accurately on the disc. During recording, the drive's laser follows this groove to ensure consistent spacing of data in a spiral track. The walls of the groove are modulated in a consistent sinusoidal pattern, so the Wobble processor can read and compare it to an oscillator for precise rotation of the disc. This modulated pattern is called a wobble groove because the walls of the groove appear to wobble from side to side. This signal is only used during recording, and therefore has no effect on the playback process. Among the DVD family of formats, only recordable media use wobble grooves.

Lossless linking describes the need to connect data streams on a disc without any unused space between the previous track and the newly recorded segment. For lossless linking, it is necessary to write data blocks in the correct position with high accuracy (within 1 micron). For this purpose, the groove is mastered with a high wobble frequency (817kHz), which ensures that the writing can be started and stopped at an accurately defined position. The writing clock as obtained from this groove is very accurate.

ADIP

Address in Pregroove is the name of the process of knowing how far into a disc the laser position is during recording. The Wobbles are counted, and an address location of the section of the disc is calculated.

The CD HF signal path and the DVD signal path needs are different. The DVD signals are handled by the Signal Processor IC for DVD Recording, the SPIDRE. The CD HF signal is handled by the Decoder, IC 7402.

Encoder/Decoder/HDR65

The Encoder/Decoder has the following functions:

- Encoder for DVD+RW. This part creates the EFM+ (16 bit) signals from the I2S data stream.
- Decoder for DVD and CD. This part processes the HF-signal from the SPIDRE. It converts the EFM(+) signals to data, and performs error detection and error correction.
- Output to SPIDRE pre-processor for RF-AGC.

This IC decodes EFM or EFM+HF signals directly from the SPIDRE. These include: HF, PLL data recovery, demodulation, and error correction.

The Encoder/Decoder has two independent microcontroller interfaces. The first is a serial I^2C bus and the second is a standard 8 bit multiplexed parallel interface. Both of these interfaces provide access to 32k of SRAM 8-bit registers for control and status.

The analog front-end input on Pins 9 and 10 converts the HF input to the digital domain via an 8-bit A/D converter. The A/D is supplied by an AGC circuit to obtain the optimum performance from the converter. An external oscillator is supplied for this subsystem to recover the data from the channel stream. It corrects asymmetry, performs noise filtering and equalization, and finally recovers the bit clock and data from the channel using a digital PLL.

The demodulator portion detects the frame synchronization signals and decodes the EFM (14 bit) and EFM+ (16 bit) data and sub-code words into 8-bit symbols. Via the serial output interface, the I^2S data (audio and video) go to the DVD+RW interface.

The spindle-motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit. The motor is a standard three phase motor. Motor speed is controlled by the Wobble Processor during record. During playback the Wobble processor is monitoring the Data stacked up in the SRAM of 7204. The Motor control signal is on Pin 98 which supplies the drive IC 7301.

AWESOME

AWESOME stands for: Adip decoding, Wobble processing, Error correction, Synchronous start/stop and Occasionally Mend Errors.

The AWESOME gate array chip, IC 7401, is a fully digital DVD+RW add-on for the HDR65. A combination of both ICs can do CD and DVD decoding and CD, DVD-R(W), and DVD+RW encoding. It contains logic for:

- Wobble processing
- Address detection
- Write clock generation
- Start and stop
- ADdress In Pregroove decoding, Adip
- Spindle motor control to do CLV on wobble
- Link bits insertion (according to DVD+RW standard).
- Output to SPIDRE pre-processor for wobble-AGC

It also receives the serial interface signal from the Encoder/Decoder IC on Pins 6, 7, and 8 and merges the internal serial bus to be sent to the analog pre-processor (SPIDRE), on pins 72, 78, and 79.

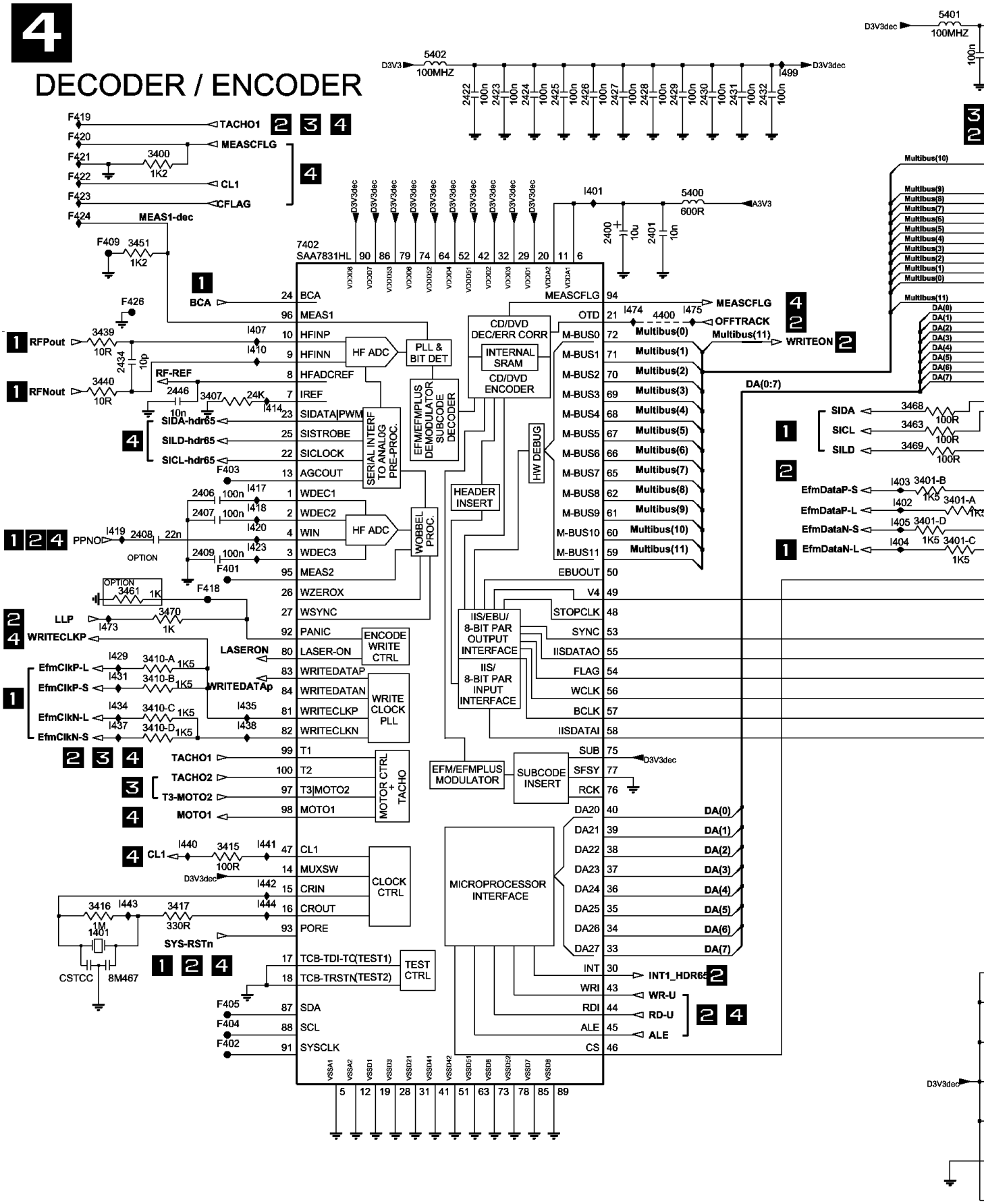
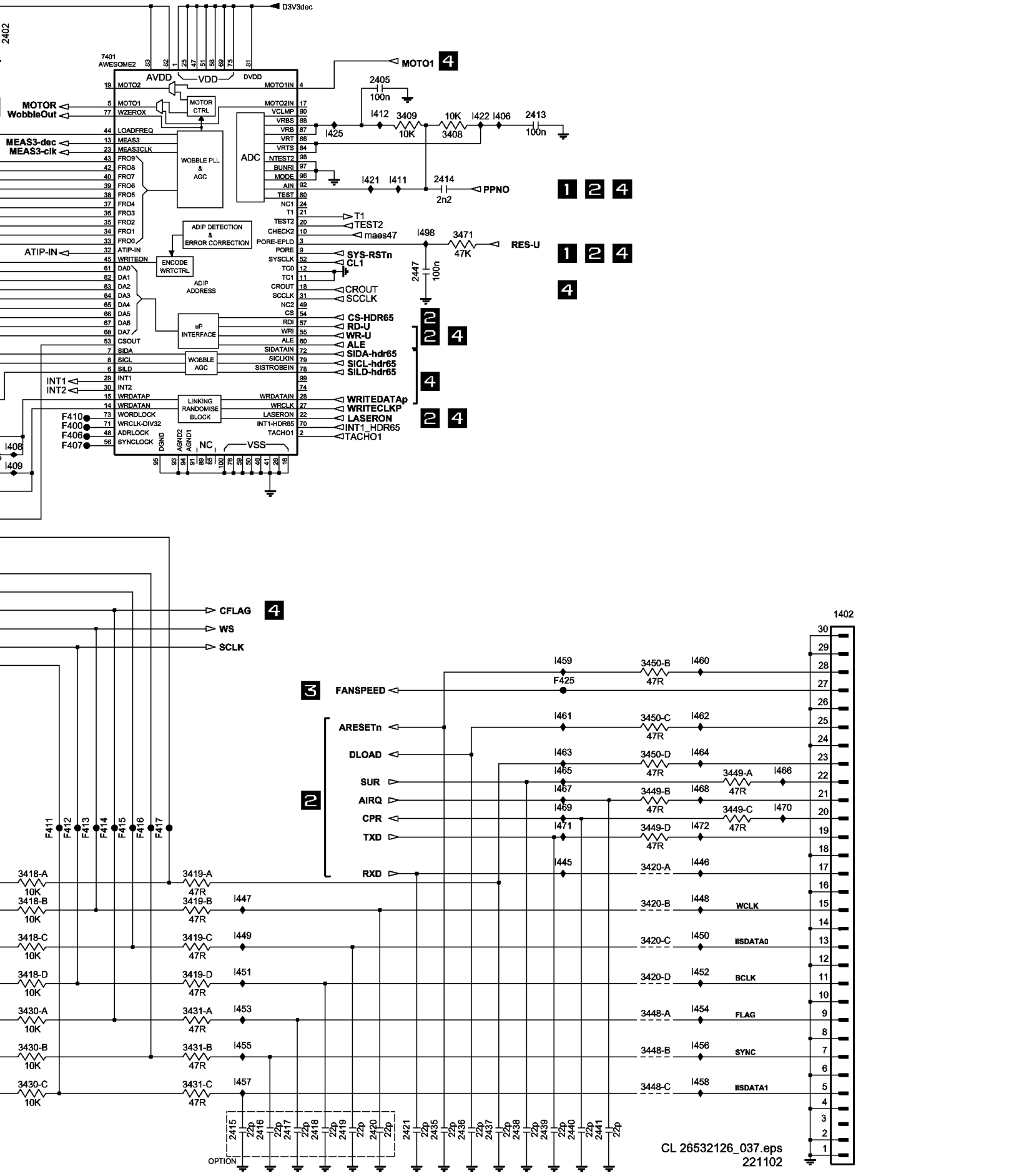


Figure 31 - Encoder/Decoder


D3V3dec
7401
AWESOME2
AVDD
VDD
DVDD
MOTO1
MOTOR
WobbleOut
MEAS3-dec
MEAS3-clk
ATIP-IN
MOTOR CTRL
WOBBLE PLL & AGC
ADC
ADIP DETECTION & ERROR CORRECTION
ENCODE WRTCTRL
ADIP ADDRESS
uP INTERFACE
WOBBLE AGC
LINKING RANDOMISE BLOCK
MOTO1
WZEROX
LOADFREQ
MEAS3
MEAS3CLK
FRO9
FRO8
FRO7
FRO6
FRO5
FRO4
FRO3
FRO2
FRO1
FRO0
ATIP-IN
WRITEON
DA0
DA1
DA2
DA3
DA4
DA5
DA6
DA7
CSOUT
SIDA
SICL
SILD
INT1
INT2
WRDATAP
WRDATAN
WORDLOCK
WRCLK-DIV32
ADRLOCK
SYNCLOCK
MOTO2
MOTO2IN
VCLMP
VRBS
VRB
VRT
VRTS
NTEST2
BUNRI
MODE
AIN
TEST
NC1
T1
TEST2
CHECK2
PORE-EPLD
PORE
SYSCLK
TC0
TC1
CROUT
SCCLK
NC2
CS
RDI
WRI
ALE
SIDATAIN
SICLKIN
SISTROBEIN
WRDATAIN
WRCLK
LASERON
INT1-HDR65
TACHO1
DGND
AGND2
AGND1
NC
VSS
2405
100n
I412
3409
10K
10K
3408
I422
I406
2413
100n
I425
I421
I411
2414
2n2
PPNO
T1
TEST2
maes47
I498
3471
47K
RES-U
2447
100n
SYS-RSTn
CL1
CROUT
SCCLK
CS-HDR65
RD-U
WR-U
ALE
SIDA-hdr65
SICL-hdr65
SILD-hdr65
WRITEDATAp
WRITECLKP
LASERON
INT1_HDR65
TACHO1
F410
F400
F406
F407
I408
I409
INT1
INT2
CFLAG
WS
SCLK
FANSPEED
ARESETn
DLOAD
SUR
AIRQ
CPR
TXD
RXD
F411
F412
F413
F414
F415
F416
F417
3418-A
3418-B
3418-C
3418-D
3430-A
3430-B
3430-C
3419-A
3419-B
3419-C
3419-D
3431-A
3431-B
3431-C
I447
I449
I451
I453
I455
I457
I459
I461
I463
I465
I467
I469
I471
I445
F425
3450-B
3450-C
3450-D
3449-A
3449-B
3449-C
3420-A
3420-B
3420-C
3420-D
3448-A
3448-B
3448-C
I460
I462
I464
I466
I468
I470
I472
I446
I448
I450
I452
I454
I456
I458
WCLK
IISDATA0
BCLK
FLAG
SYNC
IISDATA1
1402
OPTION
2415
2416
2417
2418
2419
2420
2421
2435
2436
2437
2438
2439
2440
2441
22p
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221102

Motor Drivers

The motor drivers each receive an error or control voltage. There are 6 motor drivers in this unit: the Focus Motor Driver, the Radial Motor drivers, the Turn table Motor Driver, the Tilt Motor driver, the Sled motor Driver and the Tray motor Driver.

Focus Motor Driver
The Focus motor is located on the OPU. It controls the up and down motion of the laser's lens. An error signal is produced by the MACE3 Microcomputer. The FO signal comes into Pin 3 of 7302. The Driver circuit amplifies the signal and converts it to a balanced output at Pins 1 and 2 of IC7302. The Output goes to the OPU.

Radial Motor Driver
The Radial motor is located on the OPU. It controls the side to side motion of the laser's lens. this is used in conjuction with the Sled Motor for tracking. An error signal is produced by the MACE3 Microcomputor. The RA signal comes into Pin 25 of 7302. The Driver circuit amplifies the signal and converts it to a balanced output at Pins 26 and 27 of IC7302. The Output goes to the OPU.

Turn Table Motor Driver
The Turn table Motor is a standard three phase motor simular to what is found in VCR capstan motor circuits.The driver IC,7301, receives two control voltages. The Motor Error signal comes into Pin 22. There is a Motor Enable switching voltage coming into Pin 23. A three phase drive signal is provided to the motor. Three hall elements feed speed and phase data back to the motor driver IC. These signals are amplified. Three FG signals are output to the Encoder/Decoder from Pins 16, 17, and 18.

Tilt Motor Driver
The Tilt Motor driver contains two signal paths. The motor has two field windings. The Tilt Motor has two error voltages supplied by the MACE3. The Tilt Output Cosine and Tilt Output Sine signals go to Pins 17 and 18 of 7306. The Signals are amplified and provided to the motor on Pins 12-5 of IC7306.

Sled Motor Driver
THe MACE3 produces the SL control voltage for the driver circuit. The Sled motor drive signal is provided to the Sled Motor by 7302. The SL signal comes into IC7302 on Pin 20. A control voltage is developed and amplifiers produce the drive voltages on Pins 17 and 18. These are connected to 1302 on Pins 7 and 8.

Tray motor Driver.
Trayin, and Trayout logic control lines are received from the MACE3 and a motor drive signal is provided to the Tray Motor. The logic control signal comes into IC7302 on Pins 15 and 16. A control voltage is developed and amplifiers produce the drive voltages on Pins 12 and 13. These are connected to 1301 on Pins 3 and 4.

3 DRIVER

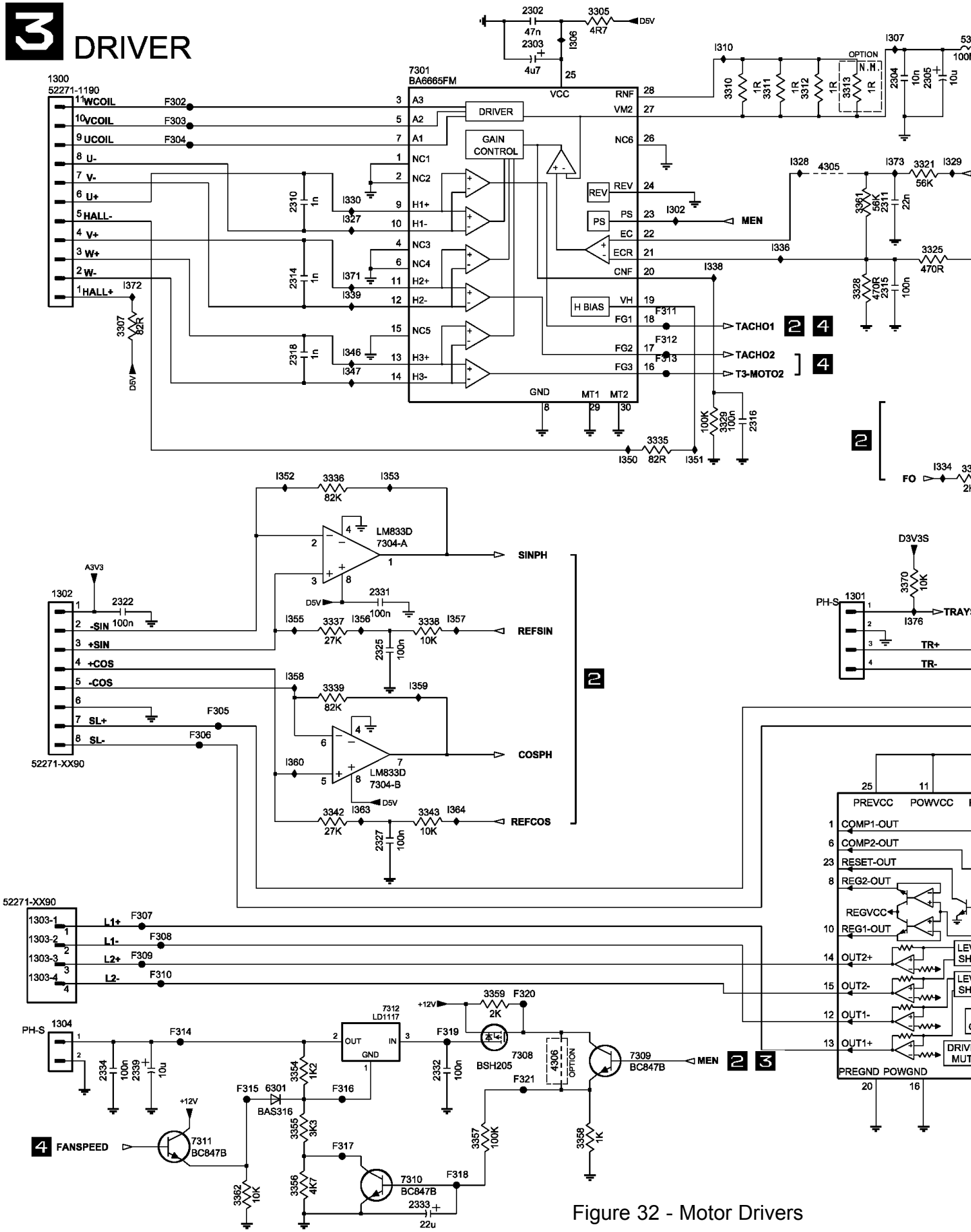
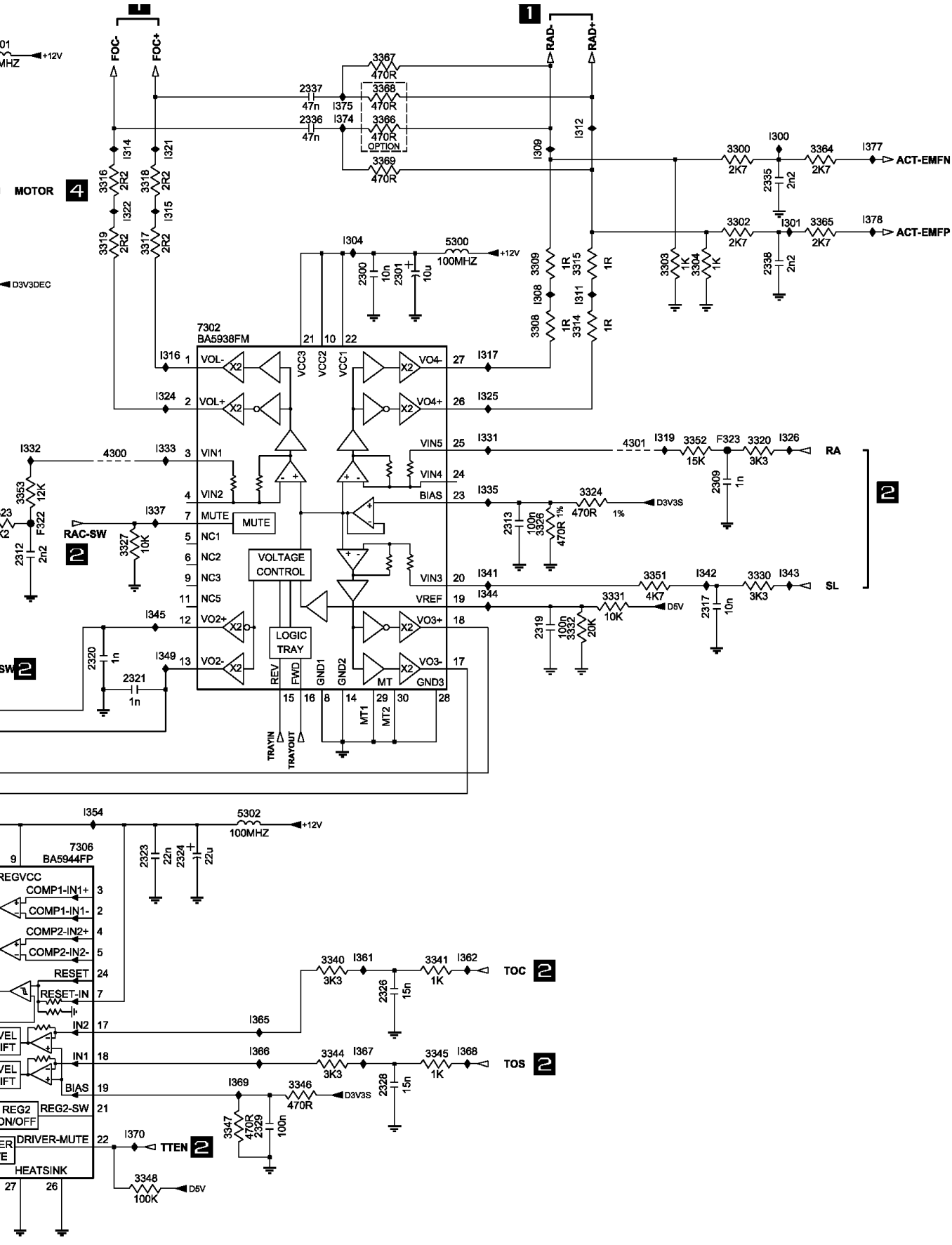


Figure 32 - Motor Drivers



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221102

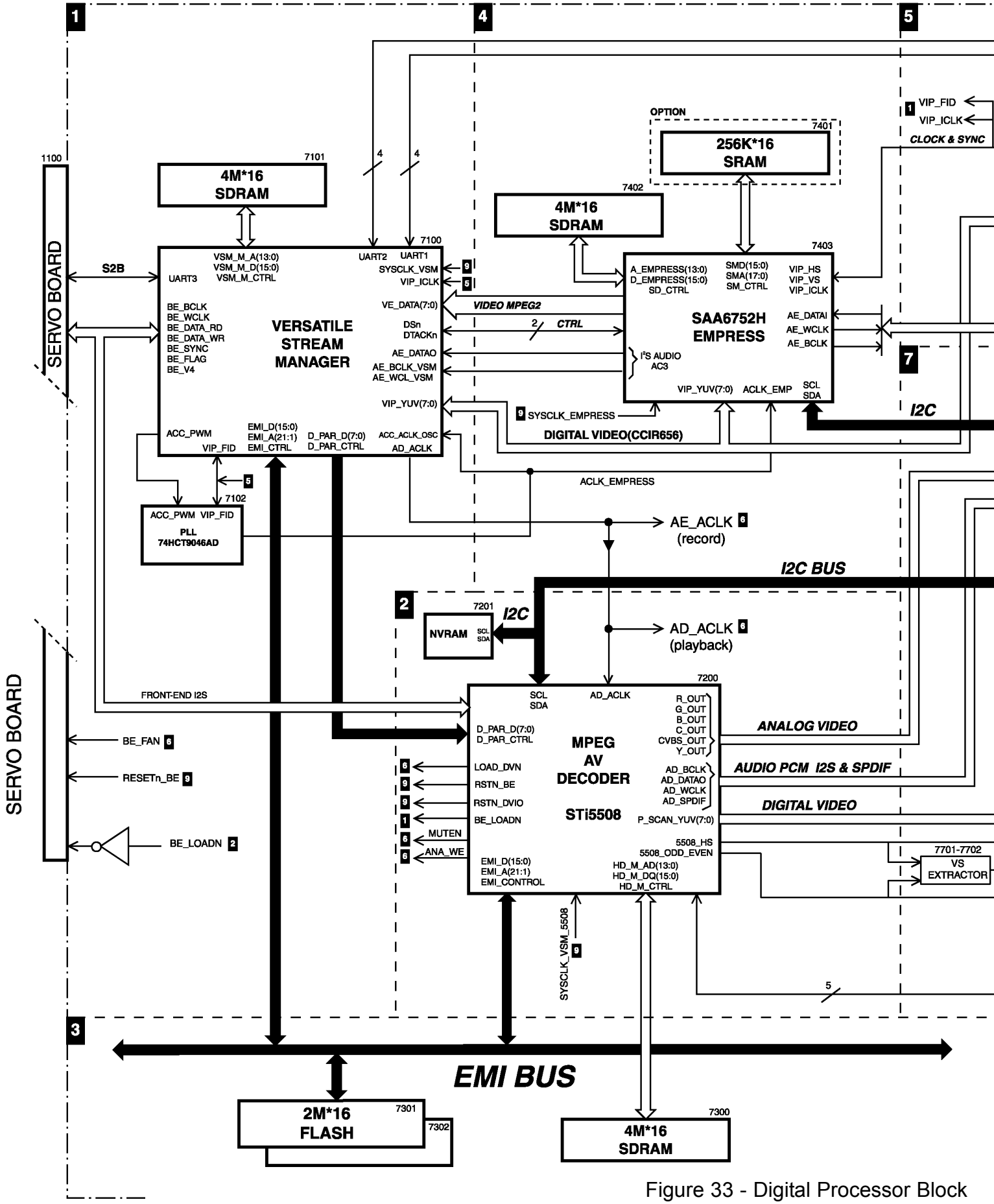
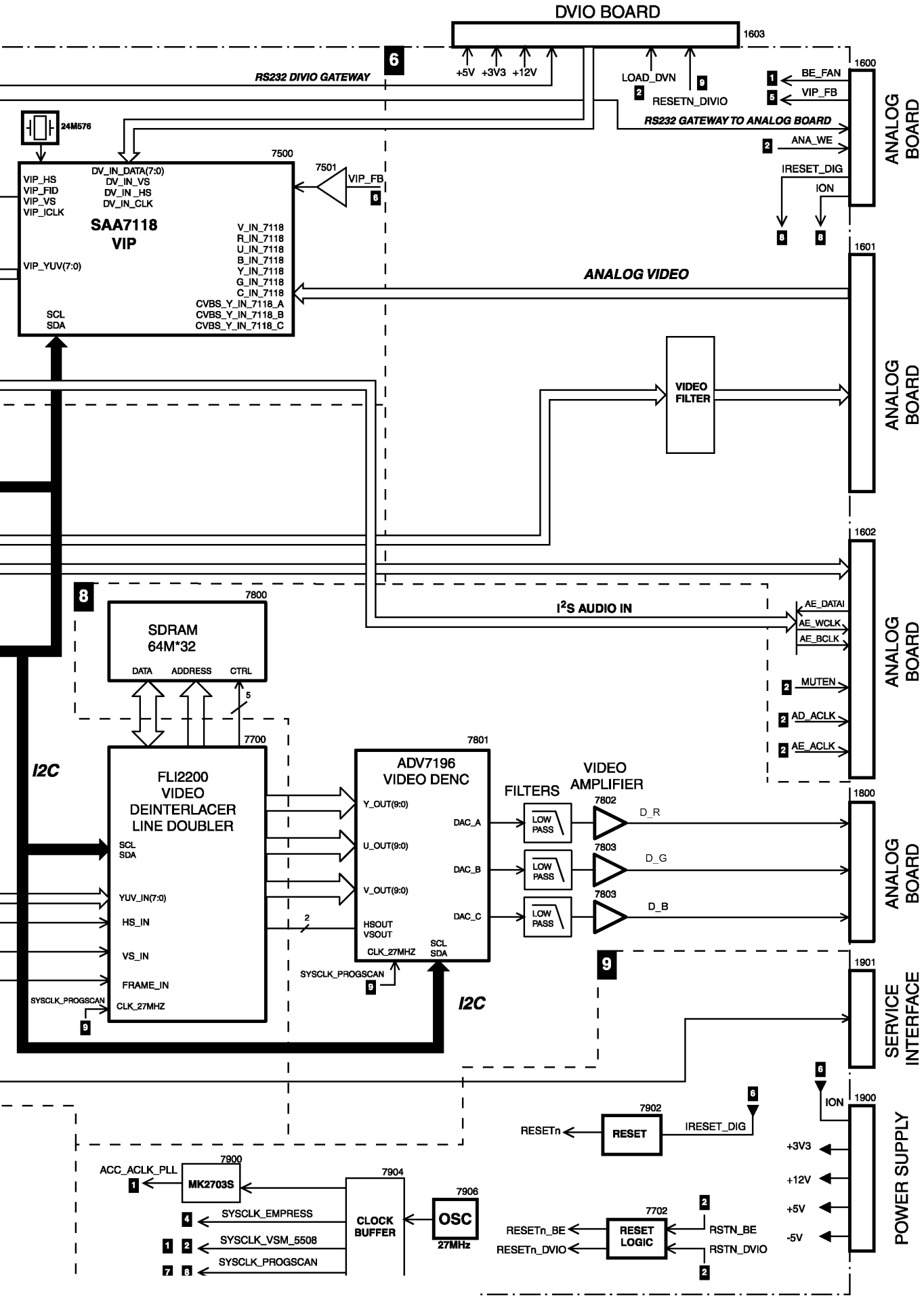


Figure 33 - Digital Processor Block


DVIO BOARD
1603
6
RS232 DIVIO GATEWAY
+5V +3V3 +12V
LOAD_DVN
RESETN_DIVIO
1600
BE_FAN
VIP_FB
RS232 GATEWAY TO ANALOG BOARD
ANA_WE
IRESET_DIG
ION
ANALOG BOARD
24M576
7500
7501
VIP_FB
DV_IN_DATA(7:0)
DV_IN_VS
DV_IN _HS
DV_IN_CLK
VIP_HS
VIP_FID
VIP_VS
VIP_ICLK
SAA7118
VIP
V_IN_7118
R_IN_7118
U_IN_7118
B_IN_7118
Y_IN_7118
G_IN_7118
C_IN_7118
CVBS_Y_IN_7118_A
CVBS_Y_IN_7118_B
CVBS_Y_IN_7118_C
VIP_YUV(7:0)
SCL
SDA
1601
ANALOG VIDEO
VIDEO FILTER
ANALOG BOARD
1602
8
7800
SDRAM
64M*32
DATA
ADDRESS
CTRL
I2S AUDIO IN
AE_DATAI
AE_WCLK
AE_BCLK
MUTEN
AD_ACLK
AE_ACLK
ANALOG BOARD
I2C
7700
FLI2200
VIDEO
DEINTERLACER
LINE DOUBLER
SCL
SDA
YUV_IN(7:0)
HS_IN
VS_IN
FRAME_IN
SYSCLK_PROGSCAN
CLK_27MHZ
7801
ADV7196
VIDEO DENC
Y_OUT(9:0)
U_OUT(9:0)
V_OUT(9:0)
HSOUT
VSOUT
CLK_27MHZ
DAC_A
DAC_B
DAC_C
SCL
SDA
SYSCLK_PROGSCAN
FILTERS
VIDEO AMPLIFIER
LOW PASS
7802
7803
7803
D_R
D_G
D_B
1800
ANALOG BOARD
I2C
9
1901
SERVICE INTERFACE
6
ION
1900
POWER SUPPLY
+3V3
+12V
+5V
-5V
7902
RESET
RESETn
IRESET_DIG
7900
MK2703S
ACC_ACLK_PLL
7904
CLOCK BUFFER
7906
OSC
27MHz
SYSCLK_EMPRESS
SYSCLK_VSM_5508
SYSCLK_PROGSCAN
7702
RESET LOGIC
RESETn_BE
RESETn_DVIO
RSTN_BE
RSTN_DVIO

Digital Signal Processor

The Digital Signal Processor has many responsibilities. Refer to **Figure 34**. It is responsible for encoding Digital Video and Audio into MPEG2 and AC3 respectively. It supplies MPEG2 and AC3 to the Basic Engine (BE) for recording. It also receives the MPEG2 Video from the BE, decodes the signal, and supplies Digital Video to the Progressive Scan circuit. It supplies Analog Video to the Analog Board, and Digital Audio (I^2S) to the Analog Board. The entire operation starts with the B+ supplies and the System Clocks.

The DVIO Board is a second source of Digital Video to the MPEG2 Encoder circuit. The Encoder circuit is contained in the EMPRESS, IC7403. The Video Input Processor, VIP, receives the selected Analog Video from the Analog Board or the DVIO Board, and converts the selected signal to digital YUV for recording.

All data going to the BE passes through the VSM. The Empress supplies MPEG2 Video to the Versatile Stream Manager, VSM. The VSM is a hub for data streams. The VSM also sends the Digital Video to be recorded back through the playback signal path. This output from the VSM is called the Parallel Digital Video path. Most of the data going to the Digital Processor from the BE goes through the VSM. The exception is the Digital Video Playback Stream. It goes directly to the MPEG2 Decoder, IC7200.

The Progressive Scan, Pscan, circuit contains a Line Doubler. The Pscan circuit sends Y/UV Digital, 480P, Video to the Analog Board to be provided to the Output Jacks.

I^2C Bus
The MPEG2 Decoder IC7200 contains a microcomputer. It communicates to the Analog Board's Microcomputer using the I^2C Bus. The I^2C bus controls the following IC's: IC7201, IC7403, IC7500, IC7700, and IC7801. The I^2C Bus is the major communication avenue for the entire unit.

EMI Bus
The VSM and the MPEG2 Decoder share a Data Bus called the External Memory Interface, EMI. The EMI contains 4 Megabytes of Flash EEPROM. The EEPROM contains the Firmware for the Digital Board.

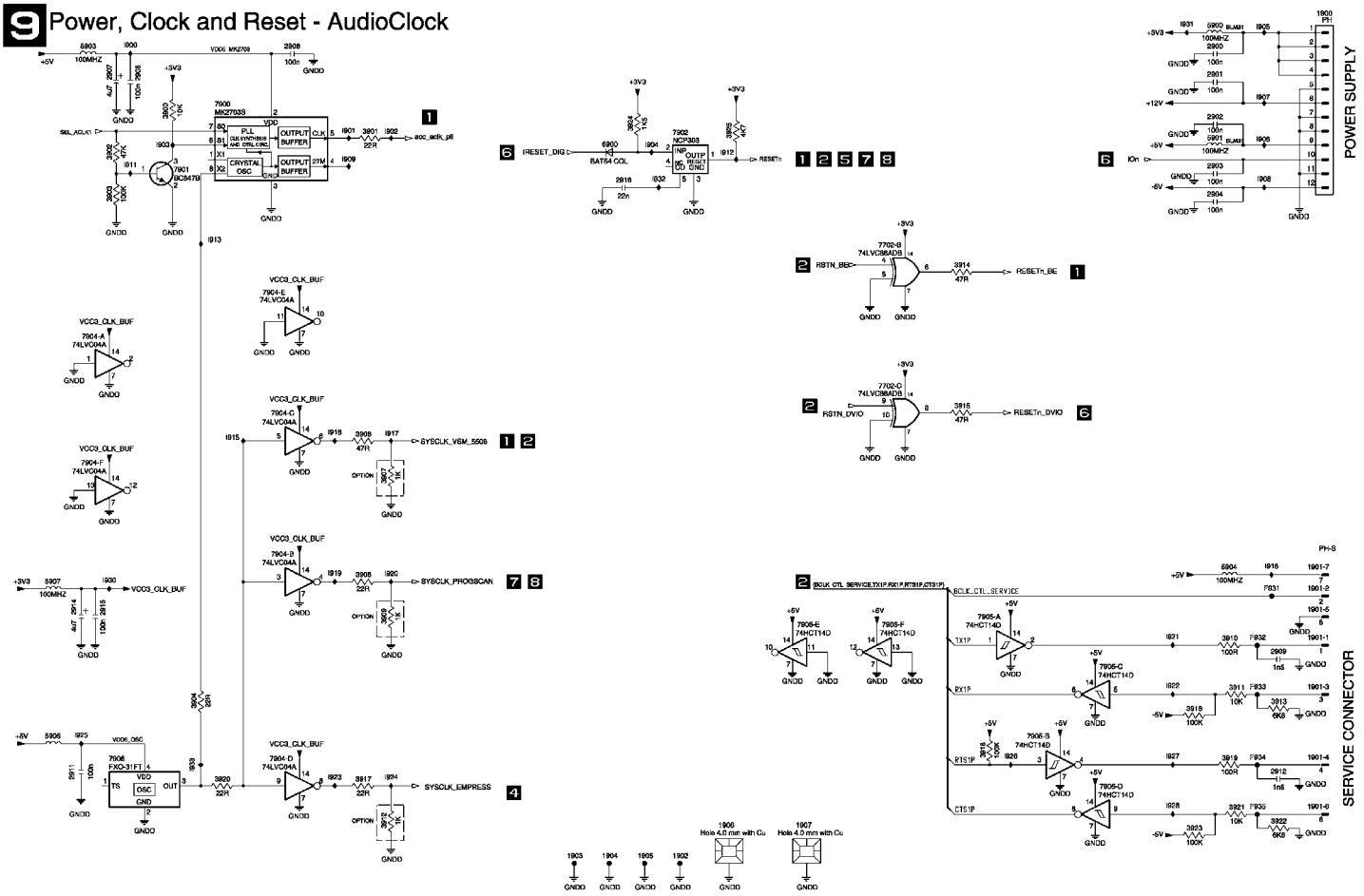


Figure 34 - Power Clock and Reset of the Digital Signal Processor

System Clocks

The System Clocks (27MHz) of the VSM, EMPRESS, and Progressive Scan circuits are generated by an oscillator, 7906. Refer to **Figure 35**. The clock signal is buffered and inverted by 7904, a quad inverter. These signals go to their respective circuits as SYSCLK_XXXX. During record mode, the audio clock, ACC_ACLK_OSC is generated by IC7102. The audio clock must be synchronized with the incoming Video Field Identifier, VIP_FID. During playback mode, the audio clock, ACC_ACLK_PLL, is generated by the clock synthesizer, IC7900. Both, ACC_ACLK_OSC (also goes to the EMPRESS as ACLK_EMP) and ACC_ACLK_PLL are fed to the VSM. The VSM selects the appropriate clock. The EMPRESS IC derives from the incoming ACLK_EMP clock the I^2S audio encoder Bit clock and Word clock, AE_BCLK and AE_WCLK. They are sent to the VSM.

On/Off

The signal IOn, coming from the Analog Board's microcomputer, enables the switched power supplies. IOn goes Low to turn power On. The switched supplies are: the 5Vdc and 12Vdc on this module.

Reset

Control signal IRESET_DIG, controlled by the microcomputer on the Analog Board is sent to the Reset Logic circuit. The IRESET_DIG transitions to High when the whole system is reset. A Low is output on Pin 1 of 7902. This signal is labeled RESETn. The n on the end of many of the names of the signal lines means enable.

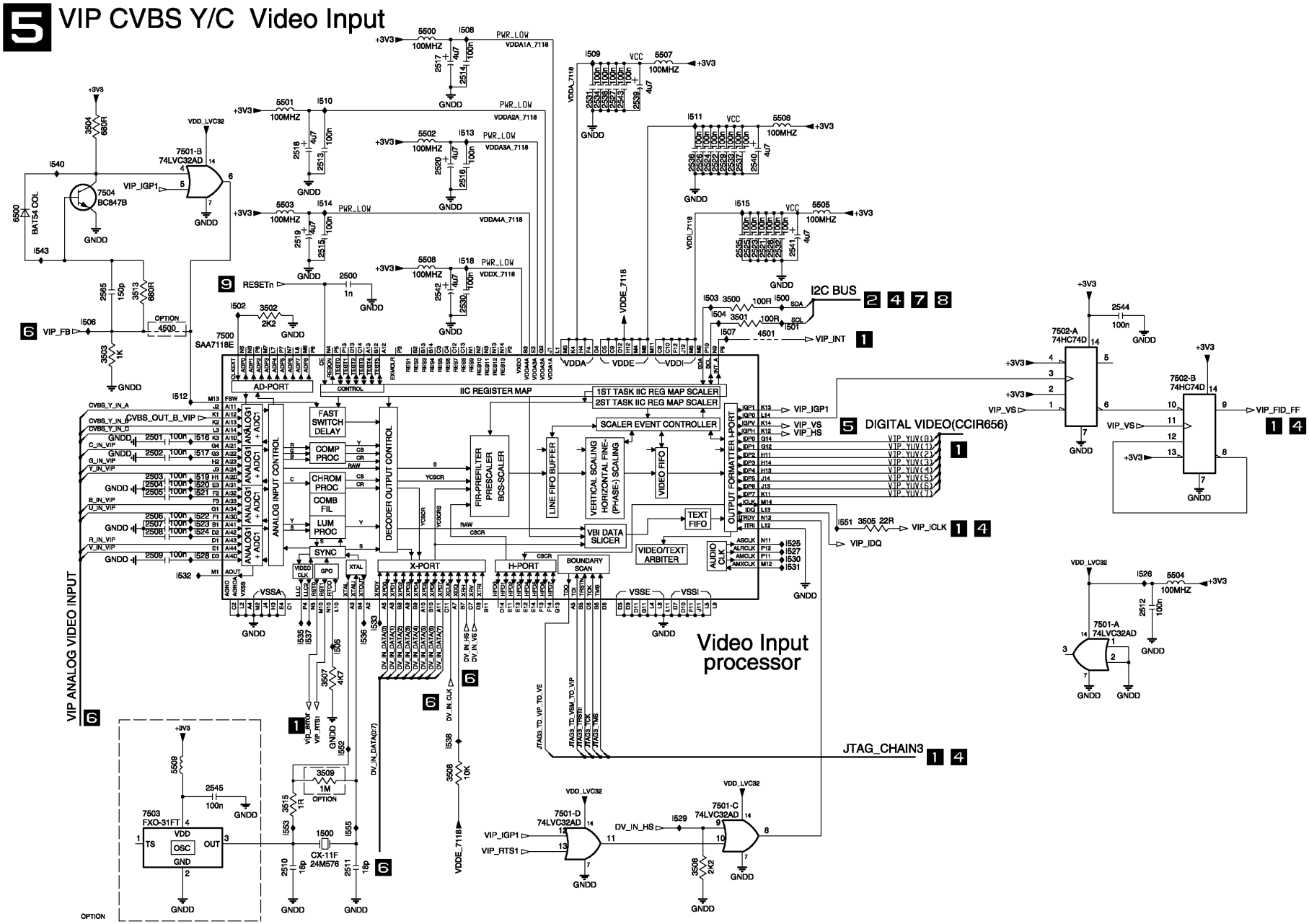


Figure 35 - Video Input Processor

Video Input Processor

Record Mode

Analog Video input signals CVBS, YC, and YUV are routed via the Analog Board to connector 1601 on Pins 14, 16, 18, 20, and 22. The signals are sent to IC7500, the Video Input Processor, VIP. If a Digital Video input source is available, 8 Digital Video input signals, DV_IN_DATA (0-7), are sent from the DIVIO Board via 1603 to IC7500. IC7500 converts the Analog Video to Digital Video. It then processes the Digital Video to comply with the CCIR656 Digital Video Stream format. The VIP IC selects between the two sources and supplies an 8 bit output stream, VIP_Y/UV (0-7). This Digital Video stream goes to IC7403/EMPRESS and to IC7100, Versital Stream Manager, VSM. The VSM uses the Digital Video for Vertical Blanking Information, VBI, extraction.

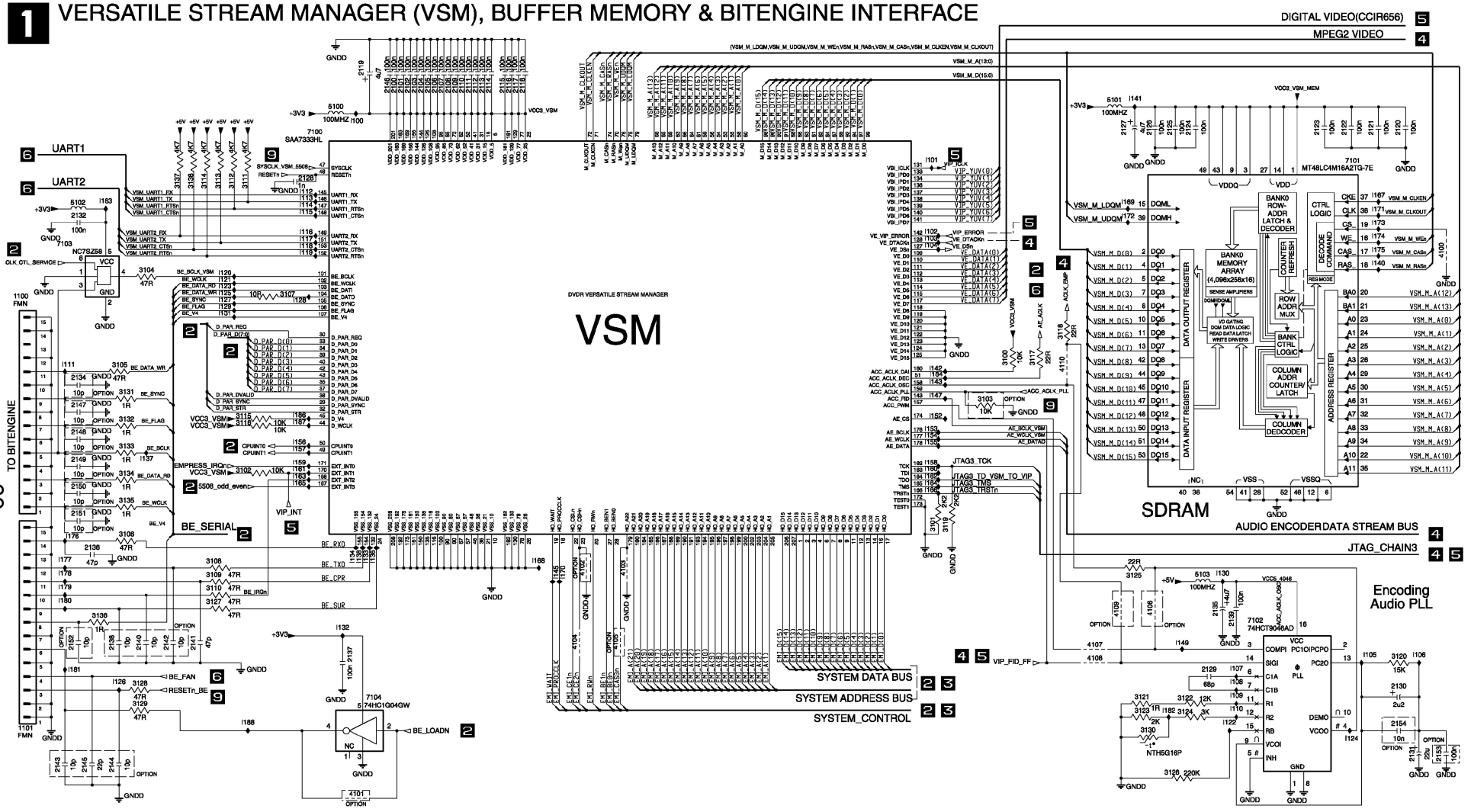


Figure 36 - Versital Stream Manager

Versital Stream Manager

The VSM is a buffer and a gateway for the data streams going to and from the Basic Engine, BE, and the rest of the data Processors. It selects which video source is to be sent to the BE for recording. The selected Video is Multiplexed with the selected Audio stream. The I^2S data containing the multiplexed data, to be recorded, goes to the BE on Pins 101-107.

The VSM must receive data from several sources. The Video comes into the VSM on two Data buses. One Data bus comes from the VIP, and the other from the EMPRESS. The SYSCLK_VSM on Pin 47 is essential for all input data processing. The VIP_FID_FF signal is necessary when the Video source to be recorded comes from the VIP. Communication on UART2 is important if the Video source to be recorded is coming from the DIVIO Board. The audio data stream coming in on Pins 177 and 178 uses two special clocks for audio. One is the AE_BCLK, and the other is ACC_ACLK_PLL..

S2B Interface
The S2B interface between the VSM (IC7100) and the Servo processor MACE3 controls the Basic Engine during record and playback mode. This serial communication goes to the BE on Pins 24, 132, 154, and 155.

Proper operation of the power up sequence involves the VSM. The VSM communicates to the Analog Microcomputer, during the Power Up Self Test operation, using UART1.

The VSM uses two types of external memories. It has dedicated SDRAM, 7101, and It shares the EMI Bus for its Firmware.

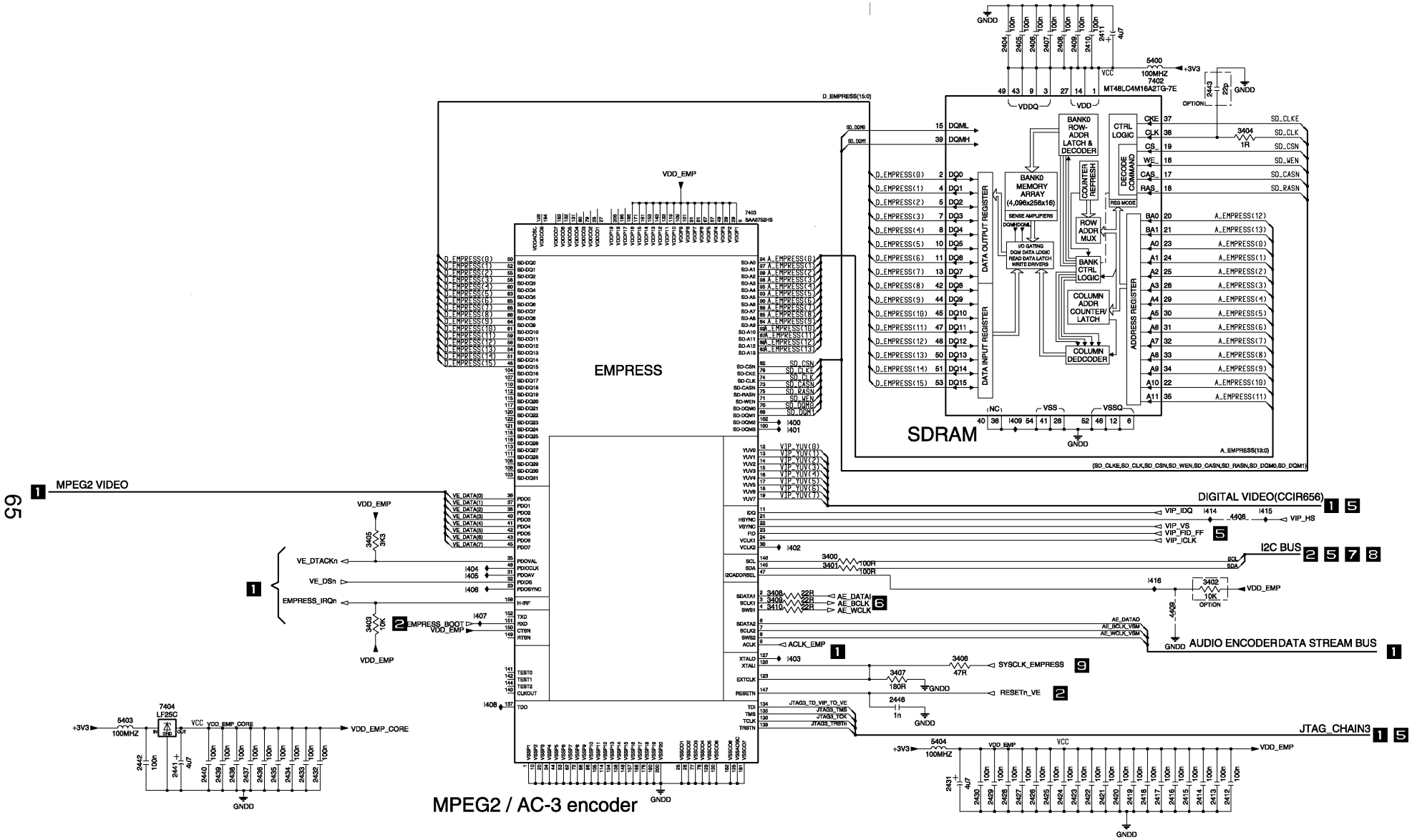


Figure 37 - Empress MPEG 2 Encoder

EMPRESS

The EMPRESS IC encodes the Digital Video stream into an MPEG2 Video stream that is fed to the VSM. Refer to **Figure 38**.

I^2S Audio is sent from the Analog Board to IC7403/EMPRESS via connector 1602. The EMPRESS compresses I^2S Audio data into an AC3 Audio stream that is fed to IC7100 (VSM). In IC7100, the Video MPEG2 stream and the Audio AC3 stream are multiplexed into an I^2S packetized stream. The serial data is sent to the Basic Engine to be recorded.

Loop-Through
The multiplexed Audio and Video stream in the VSM is fed back via the Parallel Front End Interface to IC7200. This IC decodes the MPEG2 stream into Analog Video and I^2S Audio. The Video and Audio signals are routed to the Analog Board via connectors 1601 and 1602. During recording, the record signals are present at the outputs of the Analog Board.

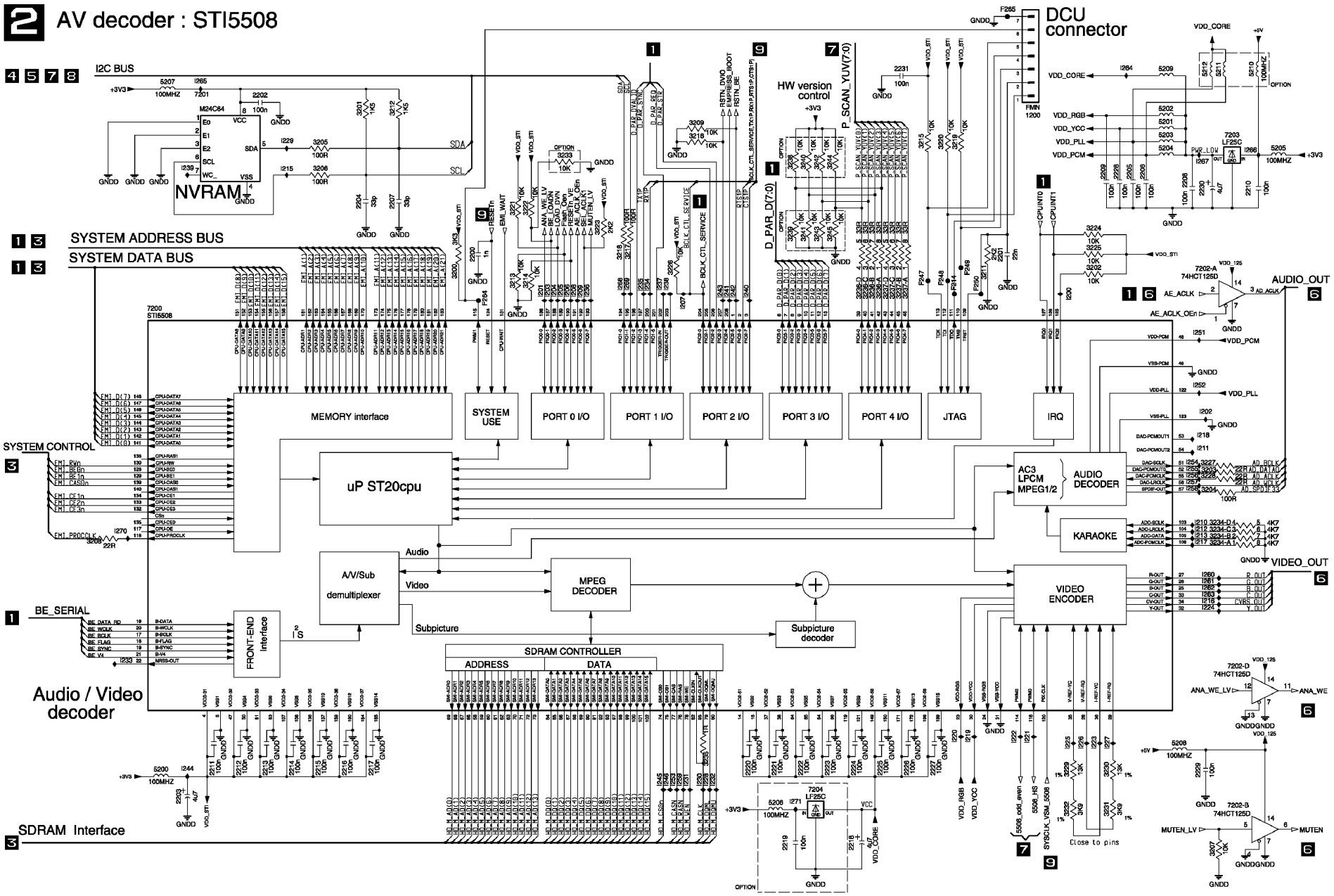


Figure 38 - MPEG2/AC-3 Decoder Circuit

MPEG2 Decoder

Playback

During playback, the serial data from the Basic Engine goes directly to the MPEG2/AC3 Decoder, IC7200 via the serial Front End I^2S Interface. Refer to **Figure 39**. IC7200 is a MPEG2 Audio/Video Decoder and has the following outputs to the Analog Board: RGB, YC, CVBS, I^2S Audio, (PCM format) and SPDIF Audio (Digital Audio output). IC7200 is the source of the I^2C bus on the Digital Board.

MPEG2 decoding is preformed in IC7200. IC7200 uses SDRAM for its many functions. The Basic Engine provides to the MPEG2 Decoder serial data from the disc on Pins 17-22. The A/V Demultiplexer separates the Audio and Video data. IC7200 also contains the analog Video Encoder. It provides RGB, Y/C and PCM audio to the Analog Board.

There is another video output path from IC7200. The Digital Video for the progressive scan circuit, PSCAN_YUV(0-7).

Record

It produces the Parallel video output path. The Parallel Video path sends the recordable video and audio back to the outputs during the record process. It receives the selected Multiplexed Data stream from the VSM via the D_PAR_D(0,7) lines. There are support signals for the Parallel Data Stream on Pins 196, 201, 205, and 206. Because of the amount of processing, the output video is delayed about 6 seconds.

ComPair

The Compair service aid connects to 7200 via a serial communication port. Using compair software and a computer's COM Port, service troubleshooting and settings can be performed. Compair has a dedicated connection on the Digital Board, 1901. The input Pins for 7200 are 2, 3, 197, 200, and, 204. Compair cannot function if 7200 does not initialize properly.

Power On

IC7200 participates in the initilazation of the unit. Power up occurs in two stages. 7200 participates in the second stage. After the Analog board and the Front Panel Microcomputer check the unit and pass their tests, the Analog Microcomputer turns On the Standby supplies. This includes the 3.3Vdc supply for 7200. 7200 then receives the DIG_Resetn signal from the Analog Board.

7200 creates three reset outputs for the Digital Boards. Resetn_VE goes to the EMPRESS. RSTN_DIVIO goes to the DIVIO Board. RSTN_BE goes to the BE. EMPRESS_BOOT signal goes to the EMPRESS for its start up flag.

If 7200 passes its self test and the other ICs communicate properly, the unit's power will stay On. If not, the unit will go into Sleep mode, never looking for keyboard input again. This process has 10 Seconds to occur. If it does not, the Analog Microcomputer will place the unit in sleep mode, turning Off the Standby supplies which is the VCC for most of the ICs on the Digital Boards.

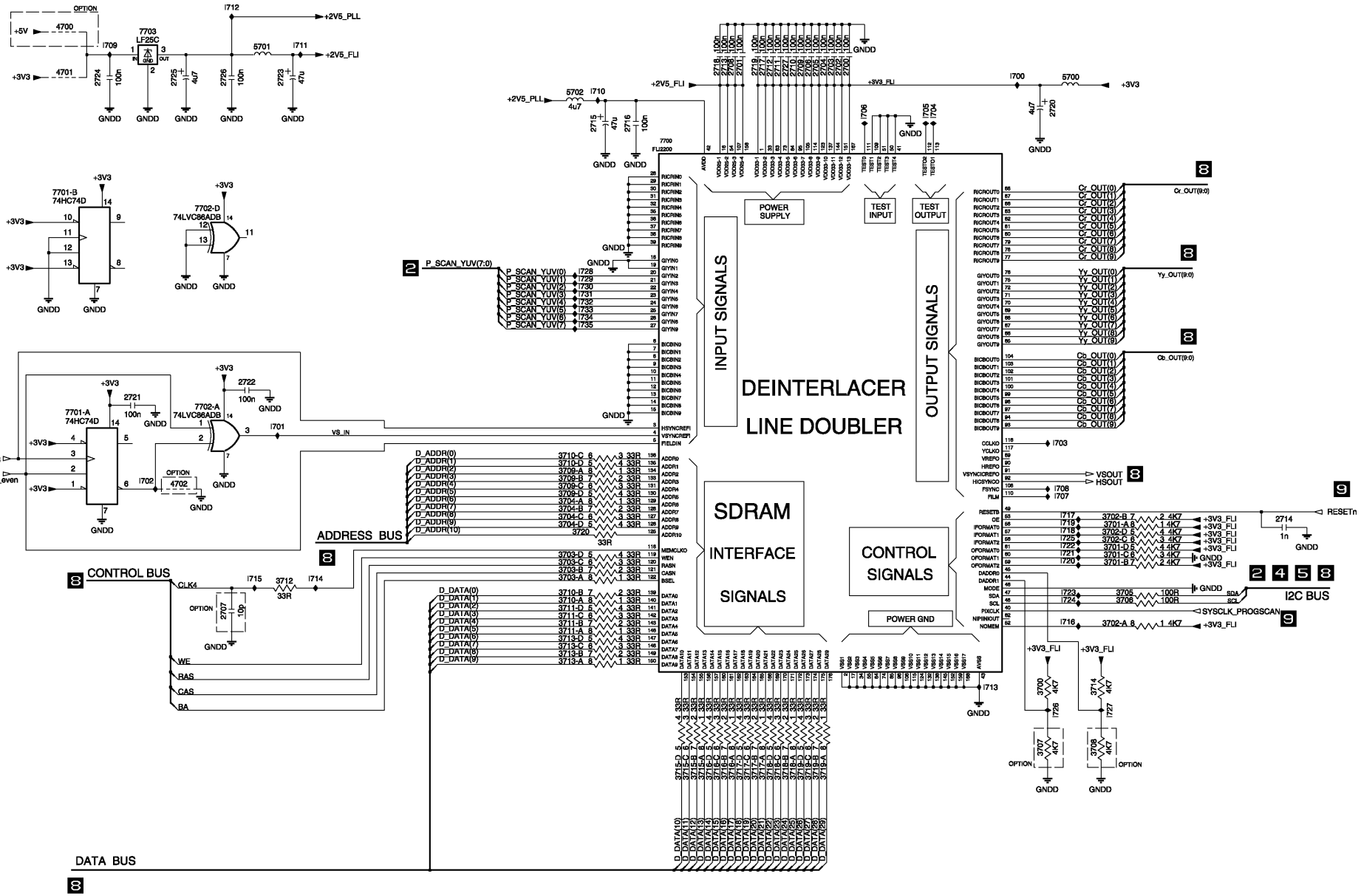


Figure 39 - Progressive Scan

Progressive Scan

The progressive scan section is integrated into the Digital Board and built around the SAGE Fli2200 Deinterlacer/Line Doubler (7700). Refer to **Figure 40**. This I^2C controlled device uses 64Mbit SDRAM (32bit x 2M) to perform high quality de-interlacing (meshing). The Deinterlacer gets his Digital YUV input data, Pins 20-27, from 7200. The format of the Digital YUV input is CCIR656 with separated H sync, V Sync. Because the 7200 doesn't have a V sync output the odd/even output of this IC has to be translated to a V sync signal. Vertical sync is generated with a flip-flop IC7701 and an XOR, 7702.

Power and Clocks
IC7701 uses two supplies, 3.3Vdc and 2.5Vdc. The system clock, SYSCLK_PROGSCAN is running at 27Mhz.

7701 produces three 8 bit output signals, Y, Cr and Cb. These are sent to the D/A converter 7801.

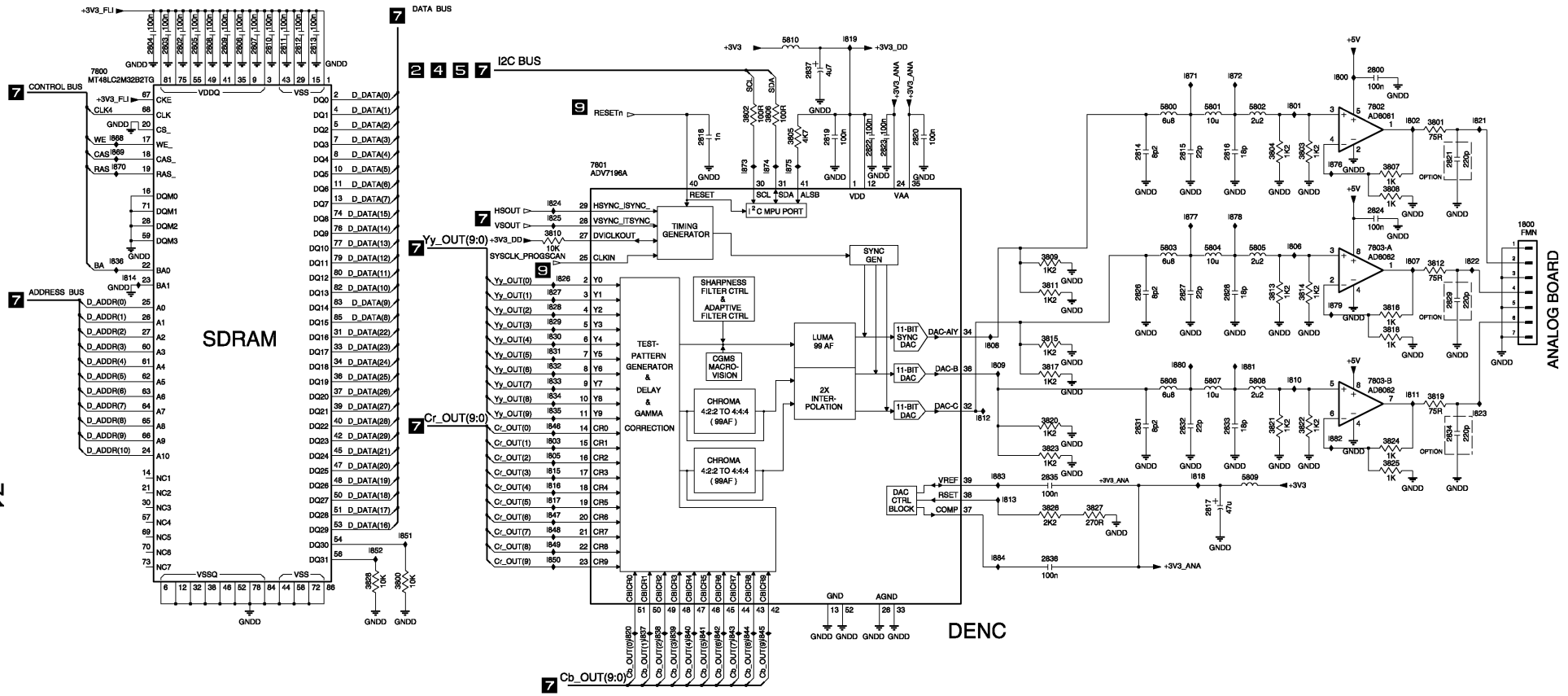


Figure 40 - Progressive Scan Output

D/A Converter

The output of 7701 (4:4:4 progressive Video) is fed to the Analog Device, 7801. The RGB output is a current signal fed via a low pass filter to the output Op Amps, 7802 and 7803. The Analog Video, 480P, is fed via a 7 poled flex to the Analog Board.

Power and Clocks
IC7801 uses the 3.3Vdc supply. The system clock, SYSCLK_PROGSCAN is running at 27Mhz.

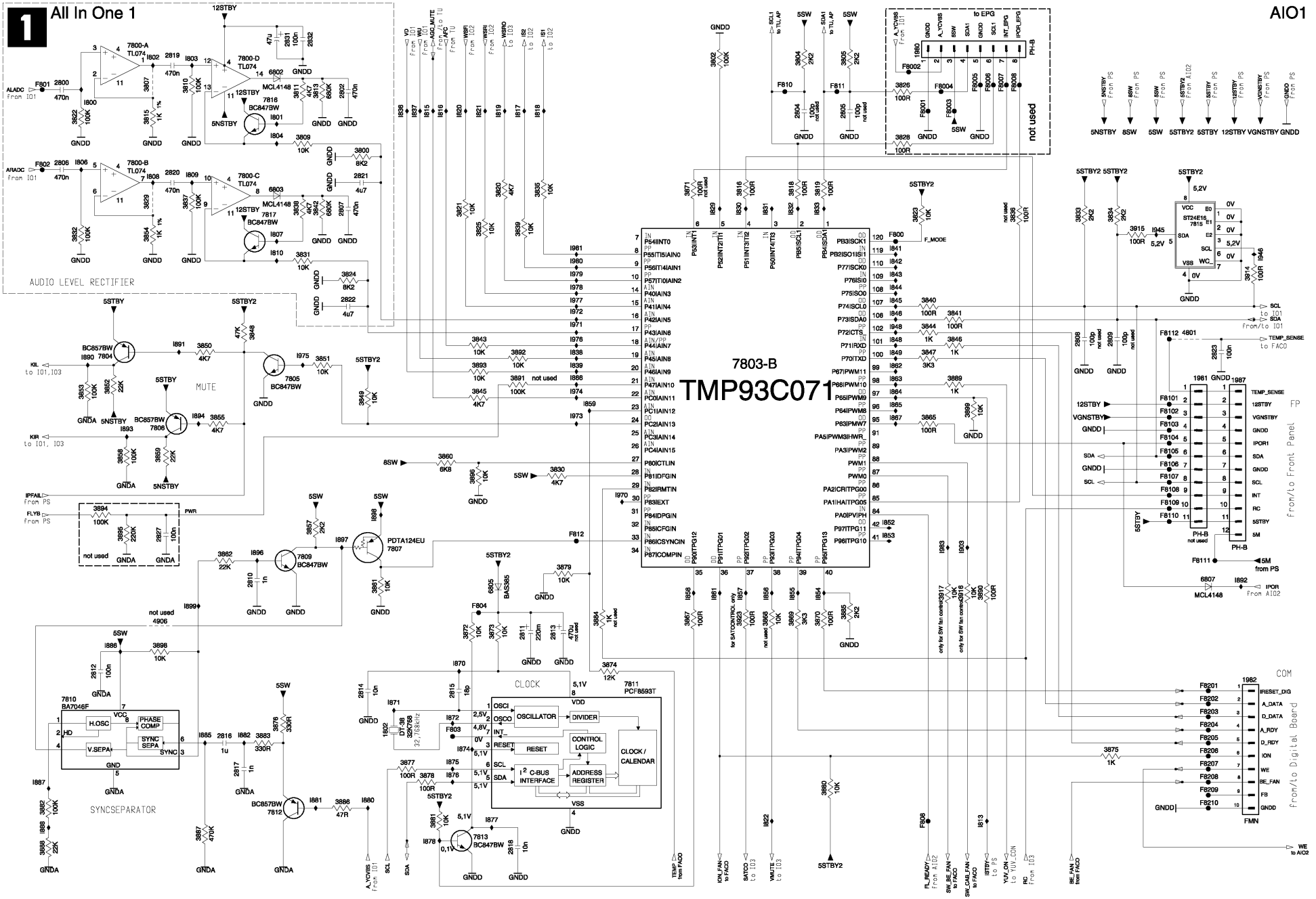


Figure 41 - Analog Microcomputer diagram 1

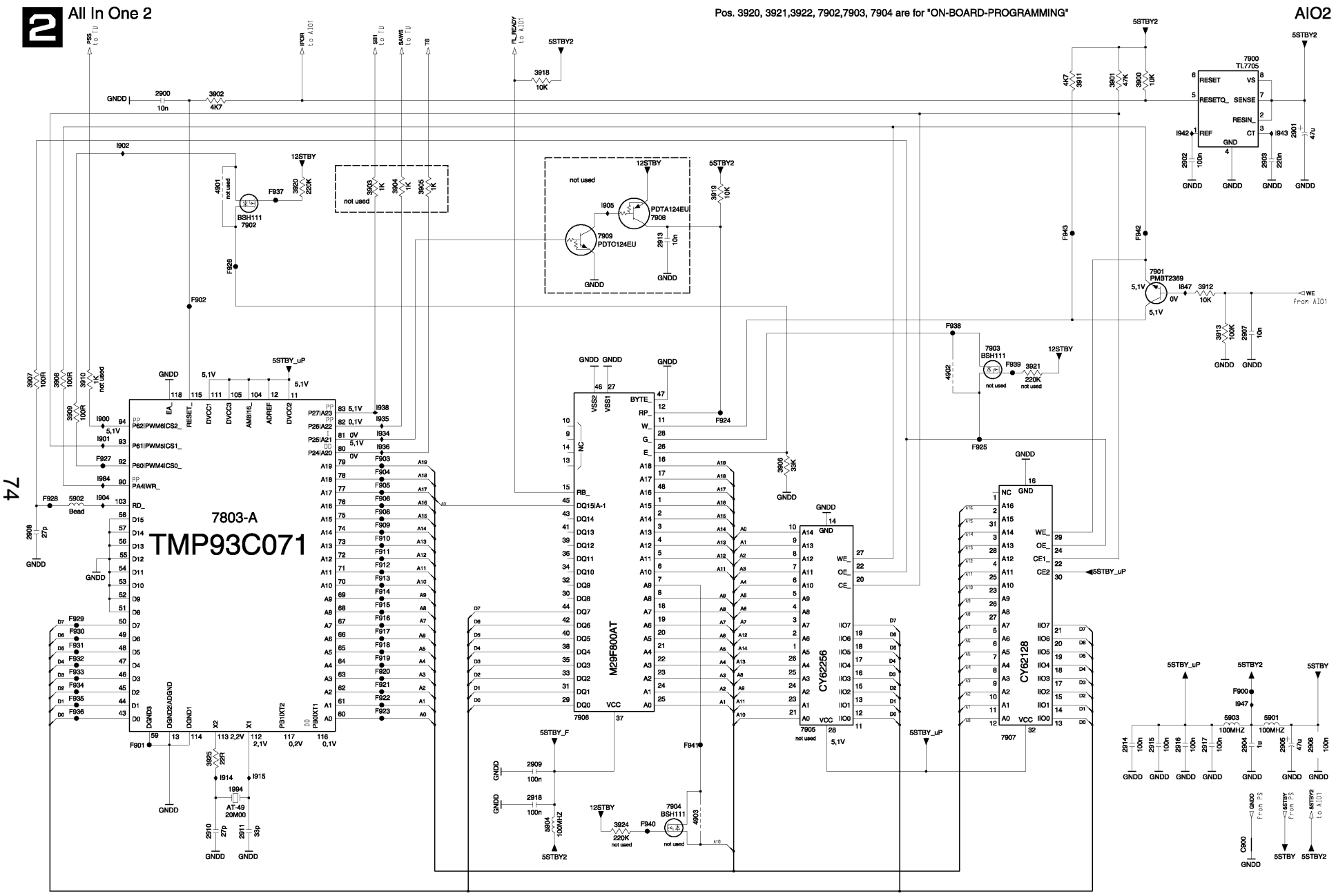


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Figure 42 - Analog Microcomputer diagram 2

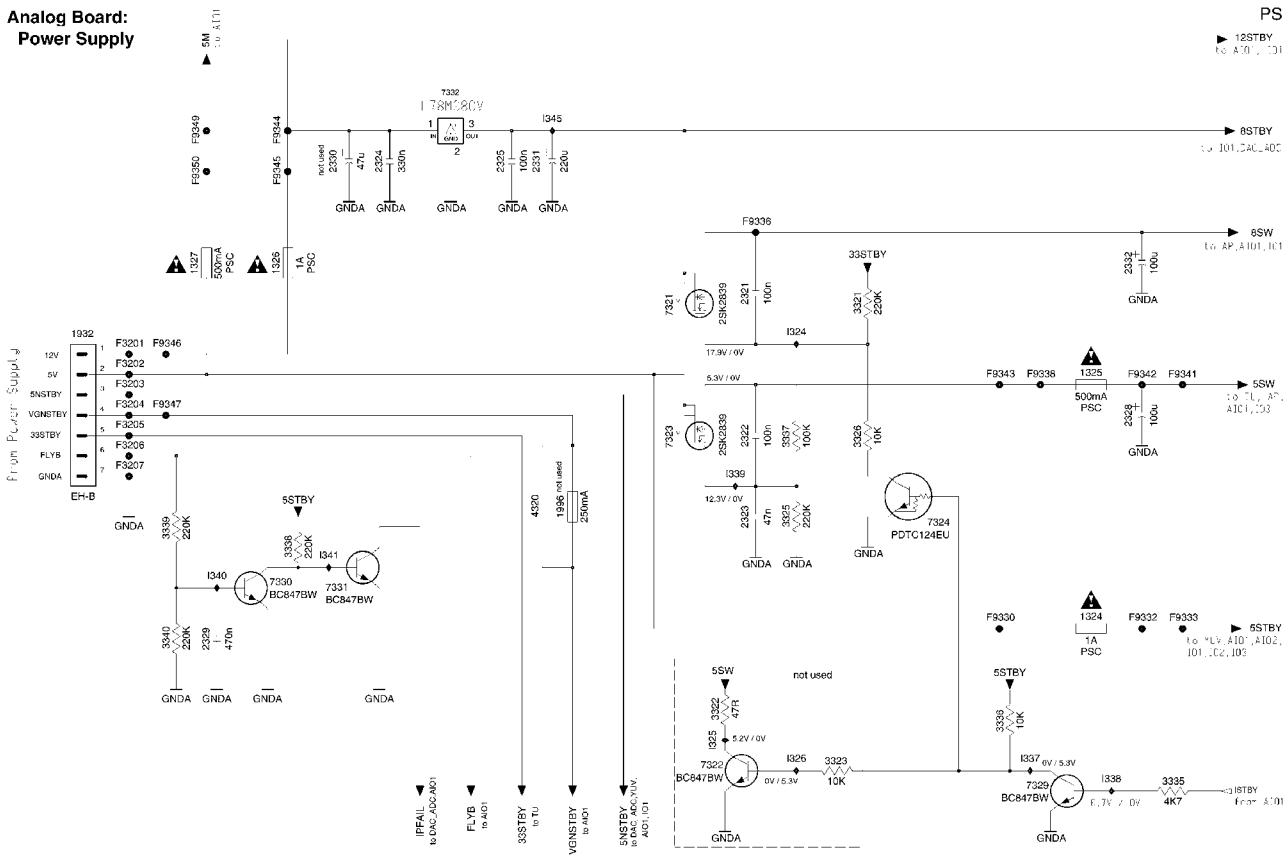

Figure 43 - Analog Board Power circuit

Analog Processor Board

The Analog Board controls all analog input/output selection, and routing. It houses the System Control Microcomputer. The System Control Microcomputer controls the routing and other functions on the board. One of its other main functions is to control power and initialization of the unit. It implements Keyboard instructions. The board has the Optical Audio Out and the Coax Digital Audio Output circuits. It controls the Tuner. The Audio D/A and A/D conversion is performed on this Board. The RGB to YUV conversion is also performed on this board. It contains the Fan Control circuit and houses the first Reset circuit for the System Control Microcomputer.

Power Supply Circuit

The Microcomputer controls the 5V Switched and 8V Switched supplies via the ISTBY line. Refer to **Figure 42**. The ISTBY line goes Low as one of the step to turn On power. When the ISTBY line goes Low, 7329 turns Off. R3336 turns On 7324. This switches 7321 and 7323 On.

There is also a power fail circuit, which is necessary to mute AUDIO when IPFAIL is low. If the FLYB line is interrupted, 7330 turns Off. R3338 turns On 7331, sending a Low to the D/A Converter to mute the Audio.

Microcomputer

The Microcomputer, IC7803, is a 16 bit processor with internal ROM and 8kB RAM. Refer to **Figures 41 and 42**. The System Clock operates at 20MHz. It uses I^2C interface to communicate with the other Microcomputers in the unit. The clock rate is approximately 95kHz. The Reset Pin is high during normal operation. It also requires a composite sync input. The microcomputer uses non-volatile EEPROM, 7815. The EEPROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc.

Power up

7803 controls power up of the unit. There are three layers to the power up sequence. The first layer involves the Analog Board and the Front Panel. The second layer involves the Digital Board and the BE. The third involves the Front Panel and the Analog Board.

The first layer controls the first set of switched supplies. After the System Control Microcomputer receives its reset, the ISTDBY control voltage goes Low to turn On the first set of switched supplies, The SW5Vdc and the SW8Vdc. It communicates on the I^2C bus initializing the Tuner, the Audio Decoder, and the Video/Audio Routing ICs. If they respond properly, It then communicates on the I^2C to the Front Panel Microcomputer. If the Front Panel Microcomputer responds properly, the ION control voltage goes Low.

The second layer occurs when the ION switching voltage comes out of the Analog Board. The ION control voltage passes through the Digital Board to the Power Supply and turns On a second set of switched voltages. These include the 3.3Vdc supply. The 3.3Vdc supply is the main B+ to many of the microcomputers throughout the unit. The System Control Microcomputer then sends out the IReset signal to 7902 on the Digital Board. This IC produces a delayed Resetn signal line for 7200. 7200 activates its I^2C and provides several reset and initialization signals for the Digital Boards and the BE. They all go through a self test. If the self test succeeds, the VSM communicates through UART1 that the system is operating, and the unit can enable the Front Panel to accept a response. The Front Panel Microcomputer then places four dashes on the Front Panel Display. ION goes High placing the unit in Standby, waiting for keyboard input. This normally takes 6-8 seconds. The System Control Microcomputer allows 10 seconds for the UART1 response. If it does not come, the unit goes into sleep mode, and will not accept keyboard input.

When the Front Panel Microcomputer receives a keyboard response, it communicates that action to the System Control Microcomputer to switch back On the second layer of switched voltages.

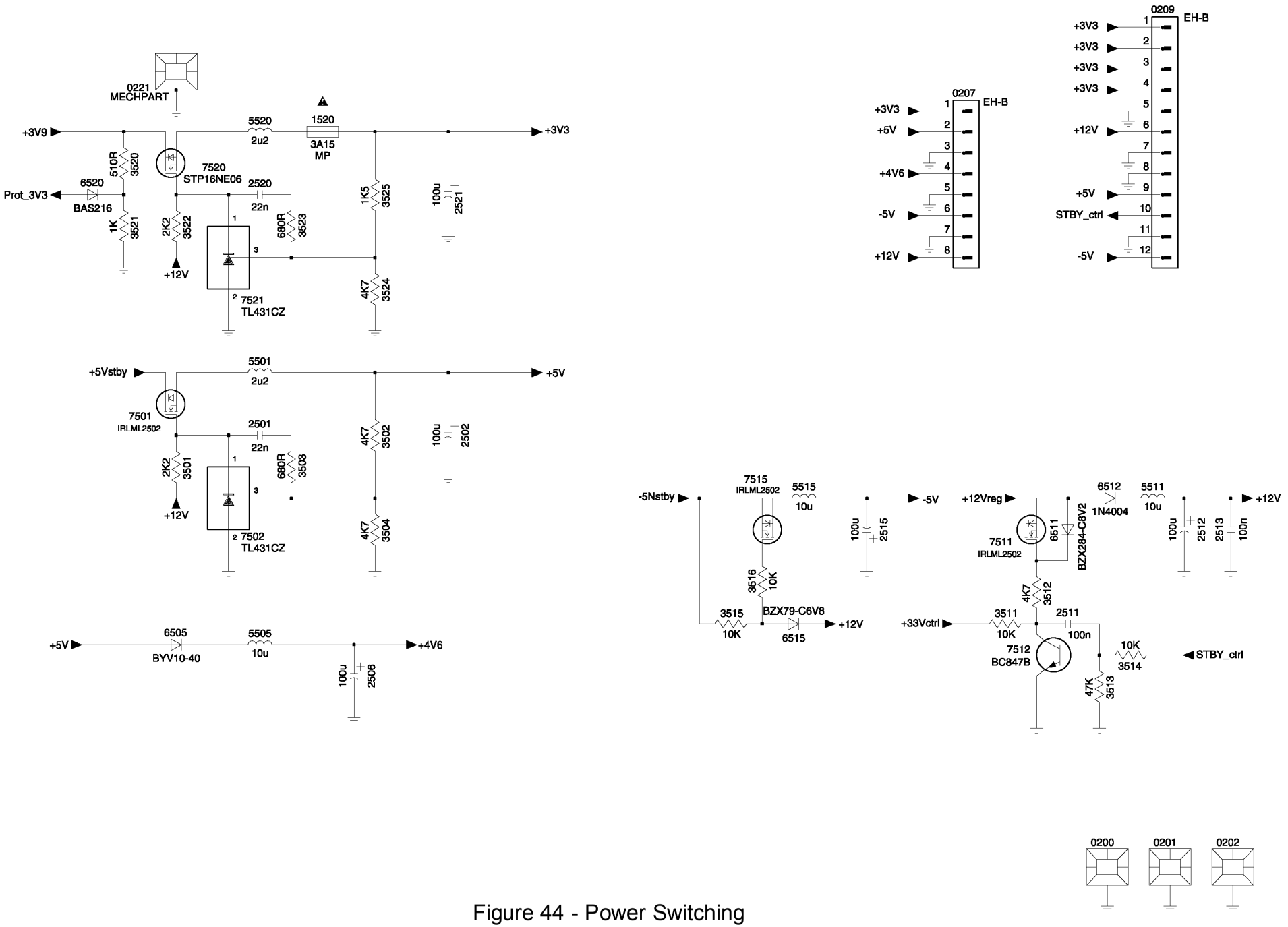

Figure 44 - Power Switching

Power Switching

The 3.3Vdc and the 5Vdc supplies are switched by the System Control Microcomputer. Refer to **Figure 44**. The 5Vdc Standby and the unswitched 3.9Vdc are supplied to two FETs, 7501 and 7520. 7515, 7511 and 7512 control 7501 and 7520. The -5Vdc Standby, the 33Vdc control voltage, and the 12Vdc regulated supplies are continuously present on 7515 and 7511. The STBY_ctrl control voltage is High when the unit is Off. The STBY_ctrl is named the ION switching voltage on the Analog Board. While the STBY_ctrl is high 7512 is biased on, keeping the Gate of the FET, 7511 Low. This keeps the 12Vdc supply Off.

When the System Control Microcomputer turns the unit On, STBY_ctrl goes Low, turning Off 7512. The 33Vdc ctrl supply supplies power to the FET, turning it On. The 12Vdc supply is present. The 12Vdc supply goes to the gates of 7501 and 7520, turning them On. The supplies to the gates are regulated by shunt regulators. The values of the monitoring resistors establish the output levels of the FETs.

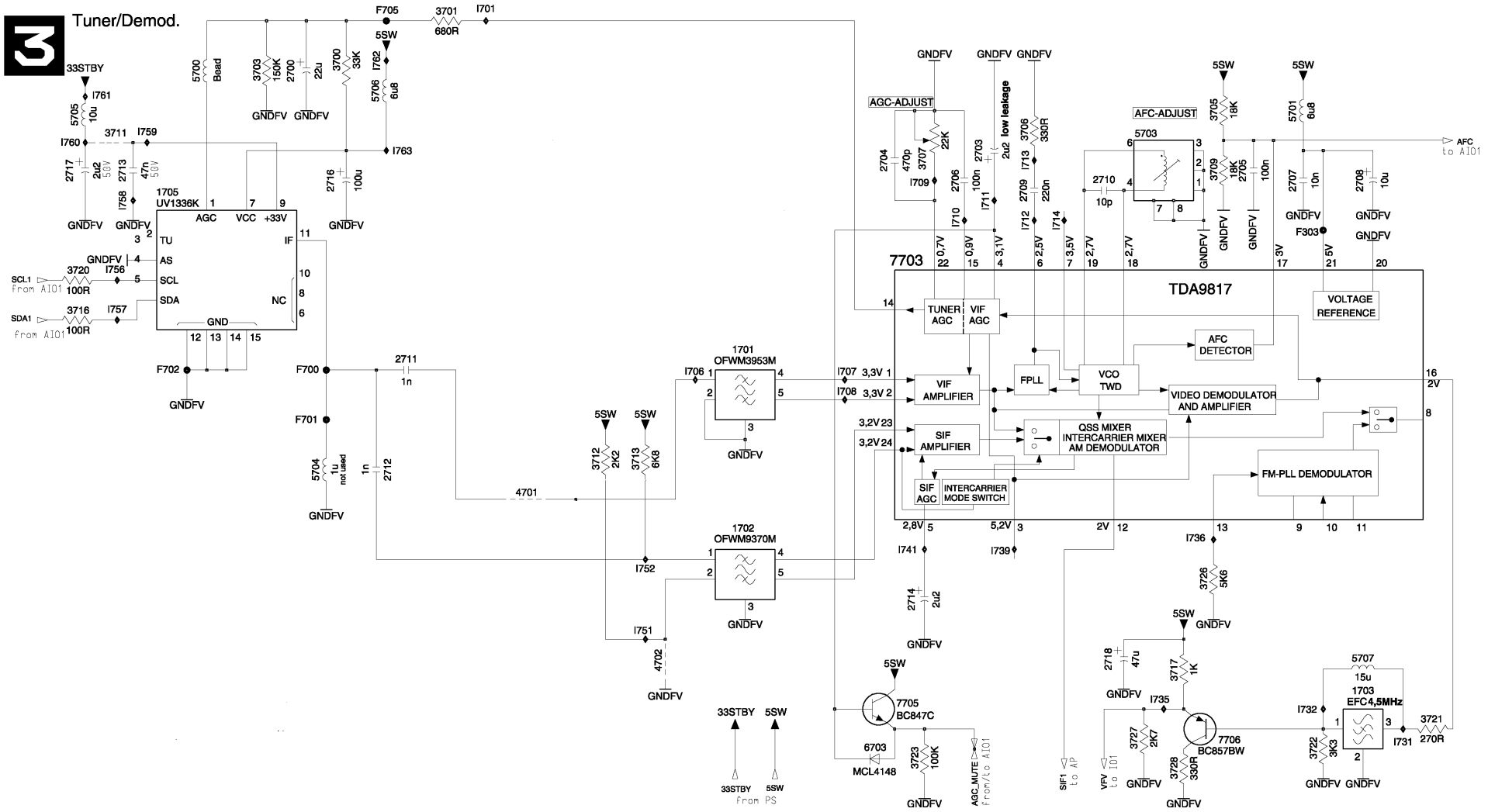

Figure 45 - Tuner Demodulator

Tuner 1705

The Tuner is capable of receiving 125 channels, and is cable ready. Refer to **Figure 45**. The RF connections on the back of the unit provide an RF loop through. There is no RF Modulator, as seen in VCRs. The Tuner/Demodulator receives two supply voltages, 33Vdc and SW5Vdc. The channel selection information is communicated via the I^2C lines.

The IF signal, from the Tuner, is processed by the demodulator, IC7703. This unit is unique in that it has two SAW Filters. 1701 is used for the Video IF, and 1702 is used for the Sound IF. The AFC coil 5703 is adjusted so that when a frequency of 45.75 MHz is supplied to the IF output of the Tuner, the AFC voltage on pin 17 of 7703 is 2.5V. The AGC is set using 3707 so that, with a sufficiently large antenna input signal (74 dBV), the voltage at the IF output of the Tuner, 1705 Pin 11 is 500 mVp-p. This adjustment must be performed with the audio carrier switched off. The demodulated Video signal appears on Pin 16 of 7703. The Demodulator AGC voltage at Pin 4 is used to determine the antenna signal strength. The FM-PLL demodulator function of 7703 is not used and is deactivated by 3726. SIF1 is generated for demodulation in the Sound processor, 7600.

The final stages in the demodulation process filter and amplify the Video. The signal is buffered by 7705, AGC_MUTE. In the opposite direction, this line may be used to mute the demodulator to avoid crosstalk when the Tuner signal is not needed. In this case, a High is sent via AGC_MUTE. The Video trap 1703 reduces adjacent channel video and any sound carrier left in the Video. The demodulated Video signal VFV is available after the buffer and limiter stage. The Limiter,7706, filters noise peaks.

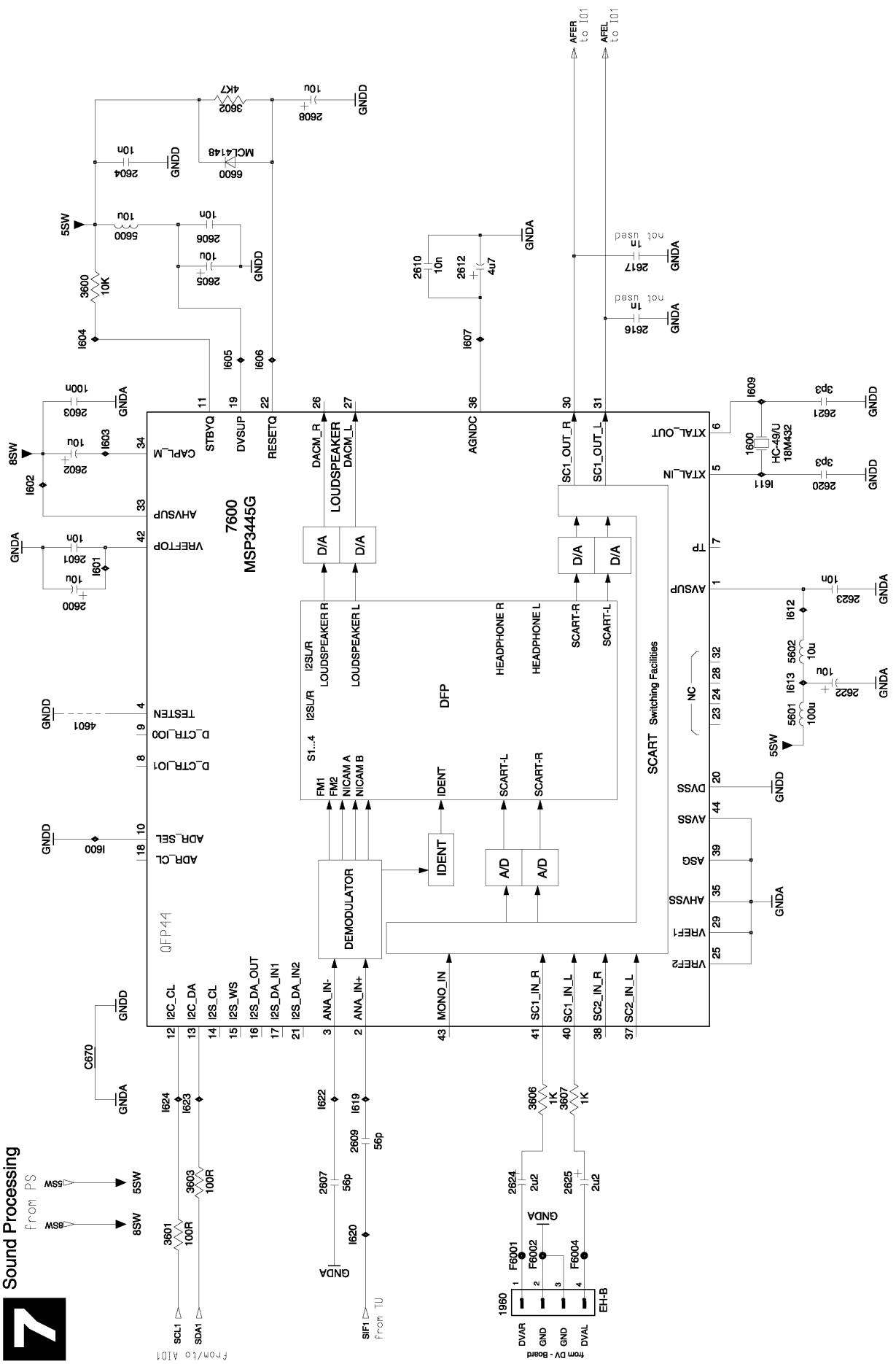

Figure 46 - Audio Demodulator

Audio Demodulator

The Sound Processor, 7600, demodulates the Audio and performs A/D and D/A conversion.

Refer to **Figure 46**. The I^2C bus controls its operation. It uses two power supplies, the 5Vdc and the 8V Switched. IC 7600 has its own oscillator on Pins 5 and 6. It is a NTSC sound processor. Amplitude and bandwidth of the demodulated Audio signals can be determined in 7600 using the I^2C bus. The Audio signal output from the Tuner is available at the Pins 30, AFER, and 31, AFEL.

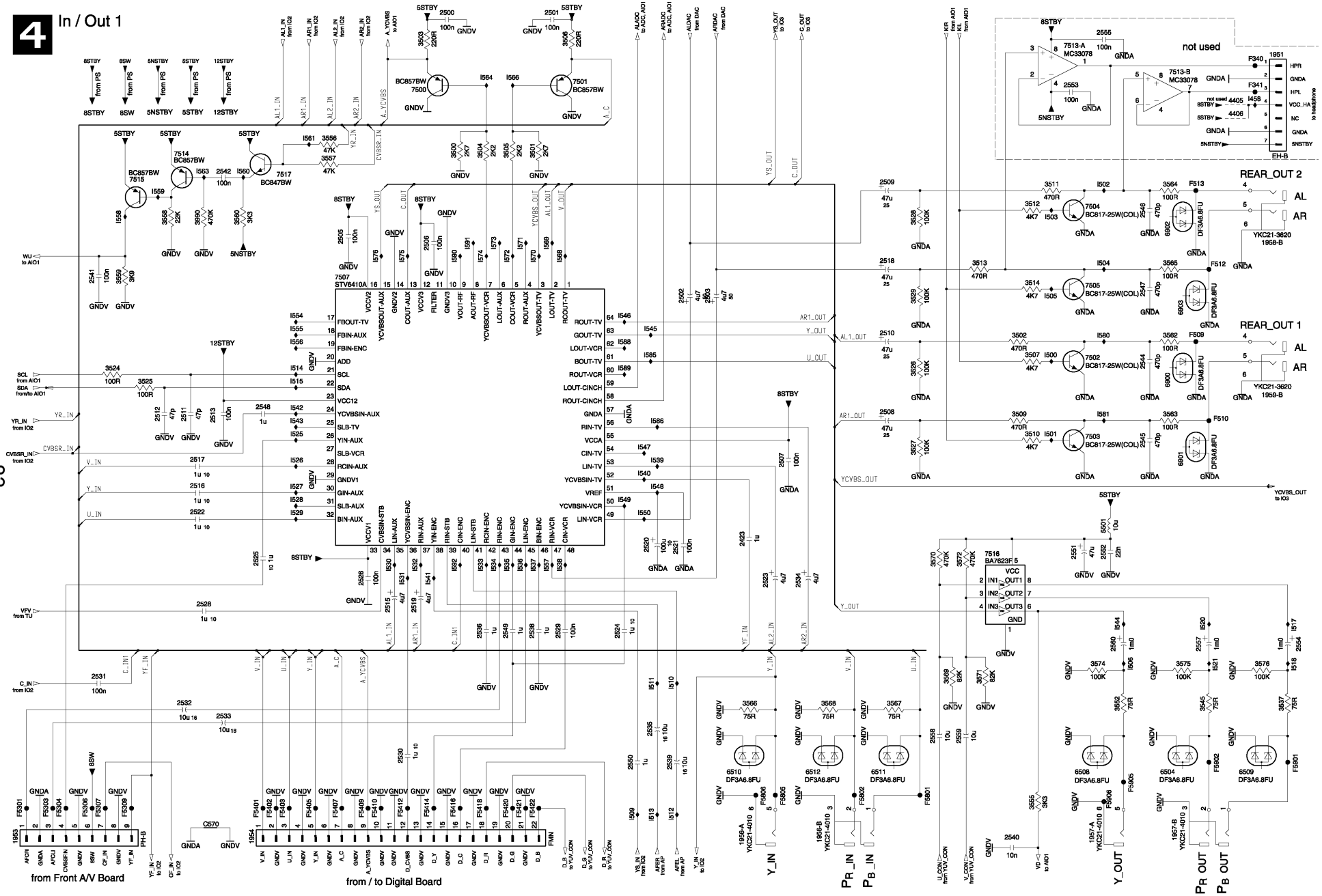

Figure 47 - Video and Audio Routing

Video and Audio Routing

The A/V I/O switching is controlled by a switching matrix, 7507. Refer to **Figure 47.** It is controlled via the I^2C Bus. 7507 has three Y, C, CVBS inputs. All switches have 6 dB amplification on the outputs.

There are two CVBS input connections possible: Front Cinch (RCA) and Rear Cinch (RCA). Both CVBS sources are connected directly to 7507 and routed to Rear Out 1 and Rear Out 2.

Figure 48 is a internal diagram for 7507.

The Audio I/O switching is also controlled by 7507 via the I^2C Bus. Analog Audio coming from Rear External Inputs 1,2, and External 3 are capacitively coupled to IC7507, Pins 35, 37, 53, and 56. Digital Board input and Tuner Audio is routed via 7600 to 7507, Pins 39 and 41. 7507 selects the audio source.

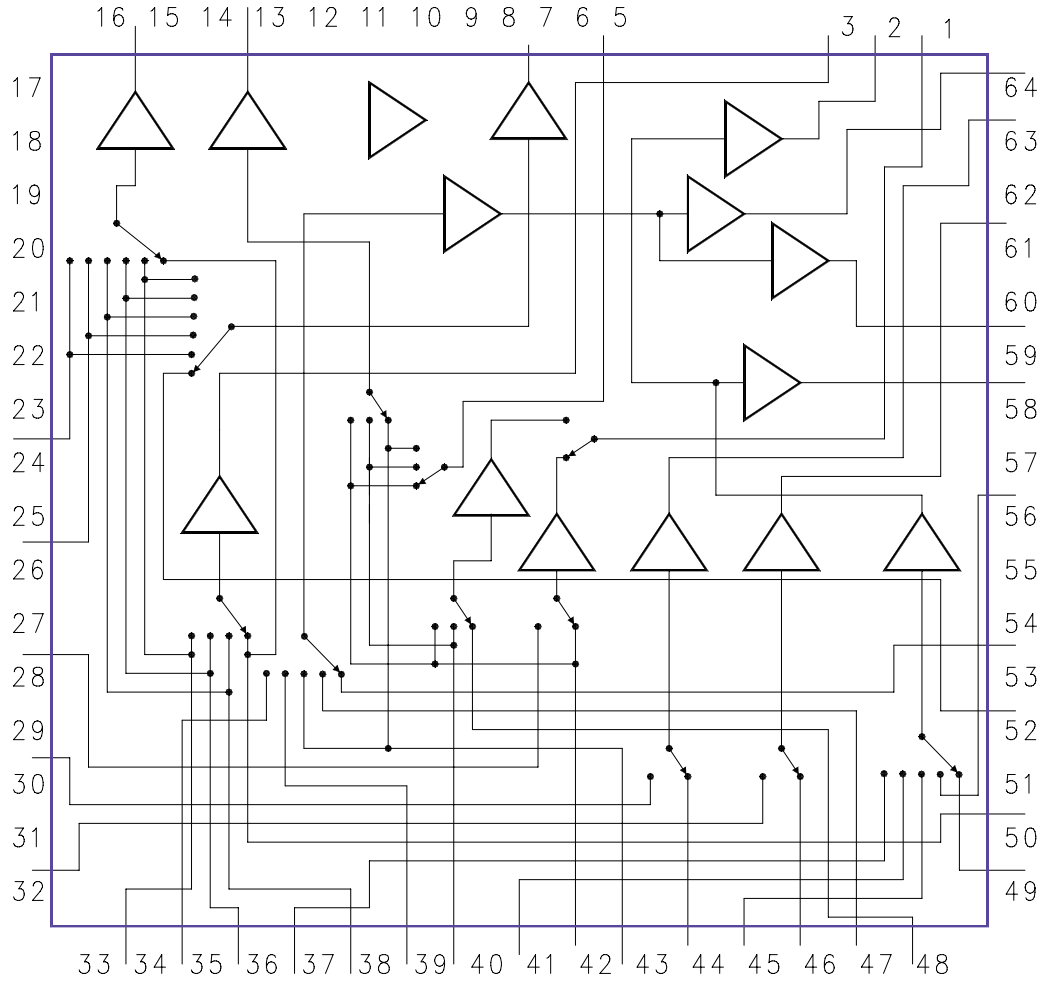

Figure 48 - IC7507 Internal Circuit

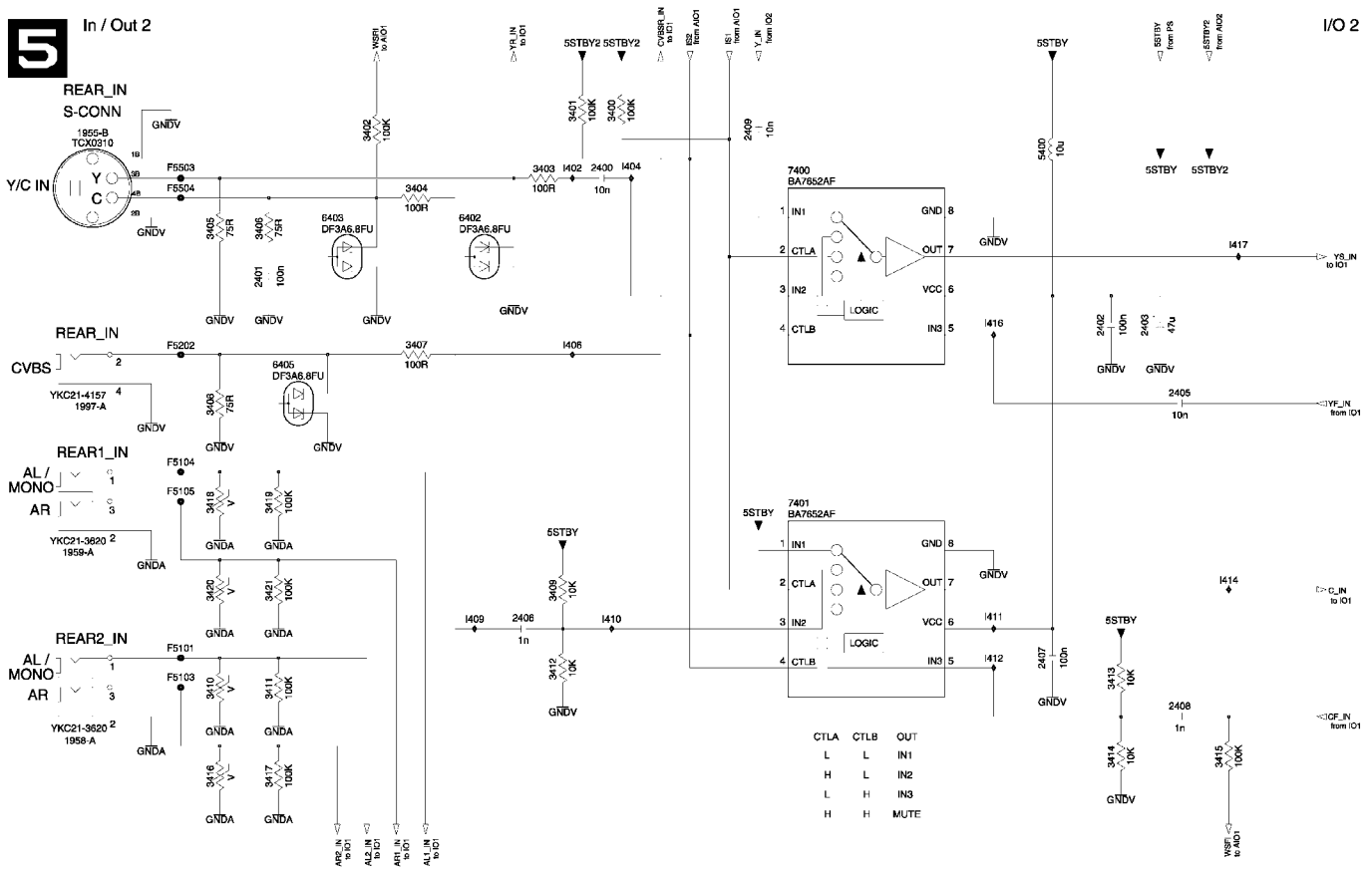

Figure 49 - Rear Input Selection

There are also two SVideo input connection possibilities: Front and Rear SVideo In, which are connected to the input selector IC 7400 and 7401. Refer to **Figure 49**. One is used for Y, the other is used for Chroma switching. The outputs of 7400 and 7401 are connected to 7507, where the signals are routed as the Y/C selected input.

Wideband Signal Selection/WSS on Y/C-Plug

Both 16 by 9 and 4 by 3 Y/C signals can be provided to the Y/C connector. The Chroma signal is sent to the Microcomputer, 7803. Pin 14 is used when using the Rear Y/C input, WSR1; and Pin 15 is used when using the Front Y/C connector, WSF1. Pin 10 of 7803 indicates which display ratio the Microcomputer is detecting. Pin 10 is Low for 4 by 3, and High for 16 by 9.

The Audio I/O switching is also controlled by 7507 via the I^2C Bus. Analog Audio coming from Rear External Inputs 1,2 and External 3 are capacitively coupled to IC7507, Pins 35, 37, 53, and 56. Digital Board input and Tuner Audio is routed via 7600 to 7507, Pins 39 and 41. 7507 selects the audio source.

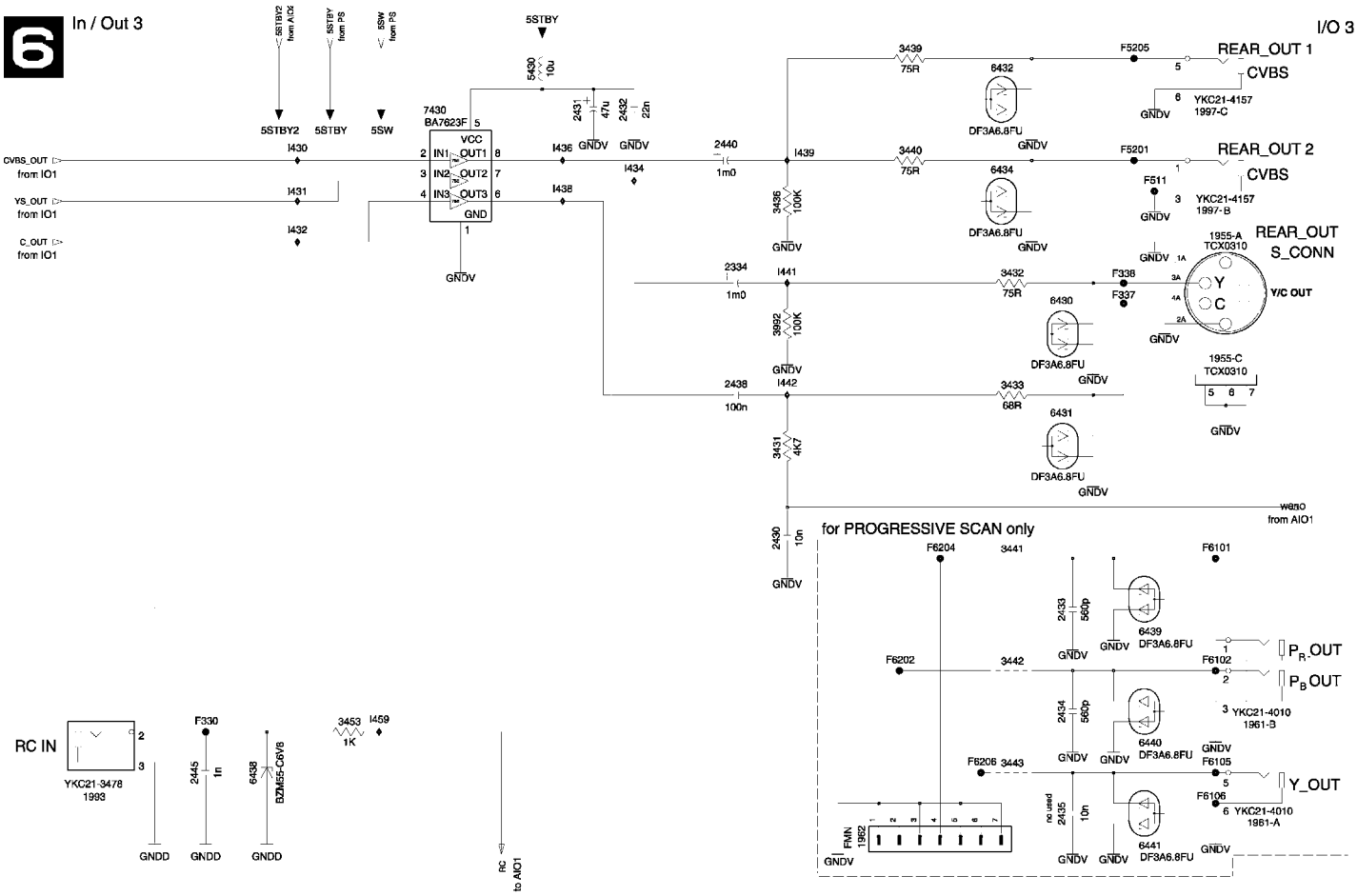

Figure 50 - Rear Output Jacks

Output Jacks

CVBS Out is provided by the 75 Ohm driver 7430. Both CVBS output sockets are connected to 7430 in parallel. Independent of which input signal is being used: CVBS, S-Video, or Y/UV, 7507 supplies SVideo and Y/UV signals to the corresponding sockets.

RC In

A Remote Control input socket is provided for those users that have a component stack with multi remote capabilities.

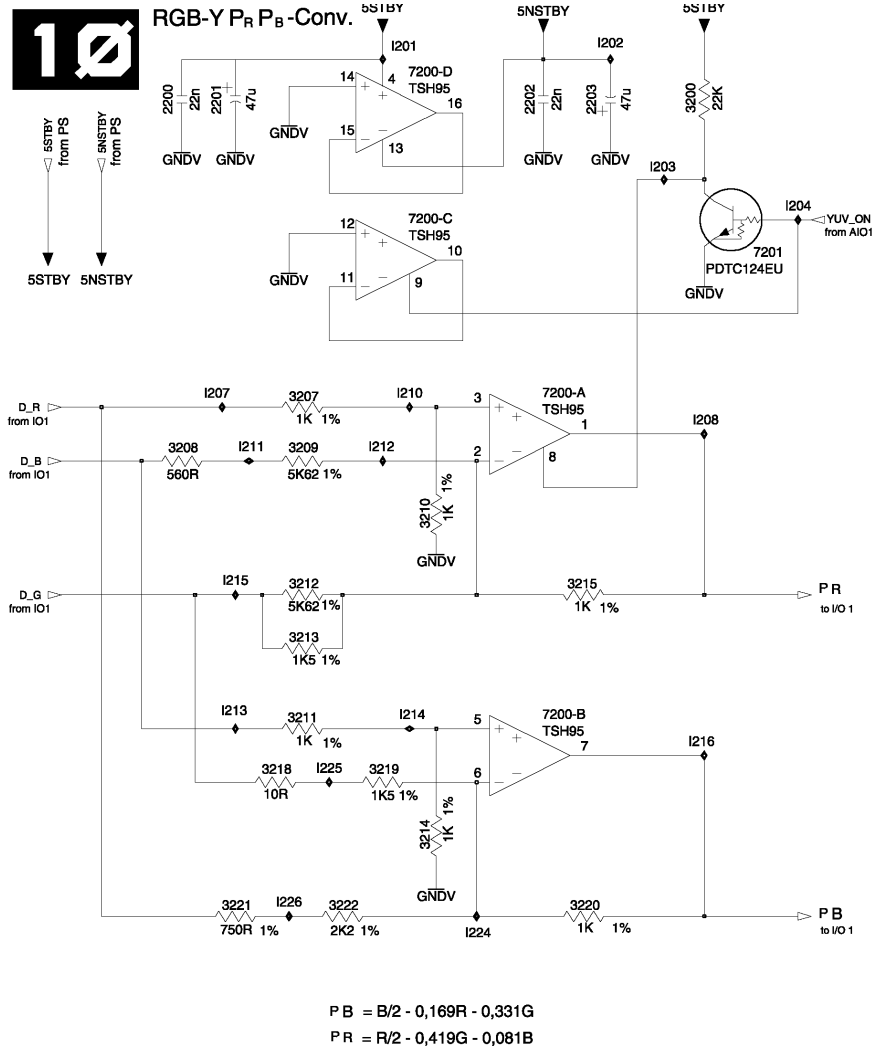

Figure 51 - RGB-Y/UV Conversion

The Y/UV In signal is routed directly to the Digital Board; there is no Y/UV IN to Y/UV Out loop through in Standby. Refer to **Figure 51**. The Digital Board supplies only RGB signals, a RGB Y/UV matrix is used. This matrix consists of the operational amplifier 7200 which generates the U and V signals according the formulas: 2U = B - .338R - .661G and 2V = R - .838G - .161B. Then the signals are routed to the UV Output sockets via the 75-Ohm driver 7516. The corresponding Y signal is coming from the Digital Board via the 7507. The 75 Ohm Y jack is driven by 7516 connected to the Y/UV Output.

Audio Conversion

Audio is converted from analog to digital for recording purposes, and digital audio is converted to Analog during playback.

A/D

This is accomplished by 7004, Refer to **Figure 52**. IC7004 uses a PCM CLK signal, a Bit CLK, and a Word CLK. An input amplitude of up to 2Vrms is expected on Pins 1 and 3. 7004 sends the data in I^2S format to the Digital Board via Pin 13.

D/A

After a delay, the processed audio data comes back from the Digital Board to a D/A converter, 7001 on Pins 10, 11, and 12. 7001 converts the I^2S data back into a balanced analog signal on Pins 28, 29, 31 and 32. IC 7001 uses a D_PCM CLK signal, a D_Bit CLK, and a D_Word CLK.

Balanced to Standard Signal Conversion

7002 converts the signals from a balanced output into standard cold ground referenced signals. The signals go to 7507 on Pins 47 and 49, and the Audio Out Jacks.

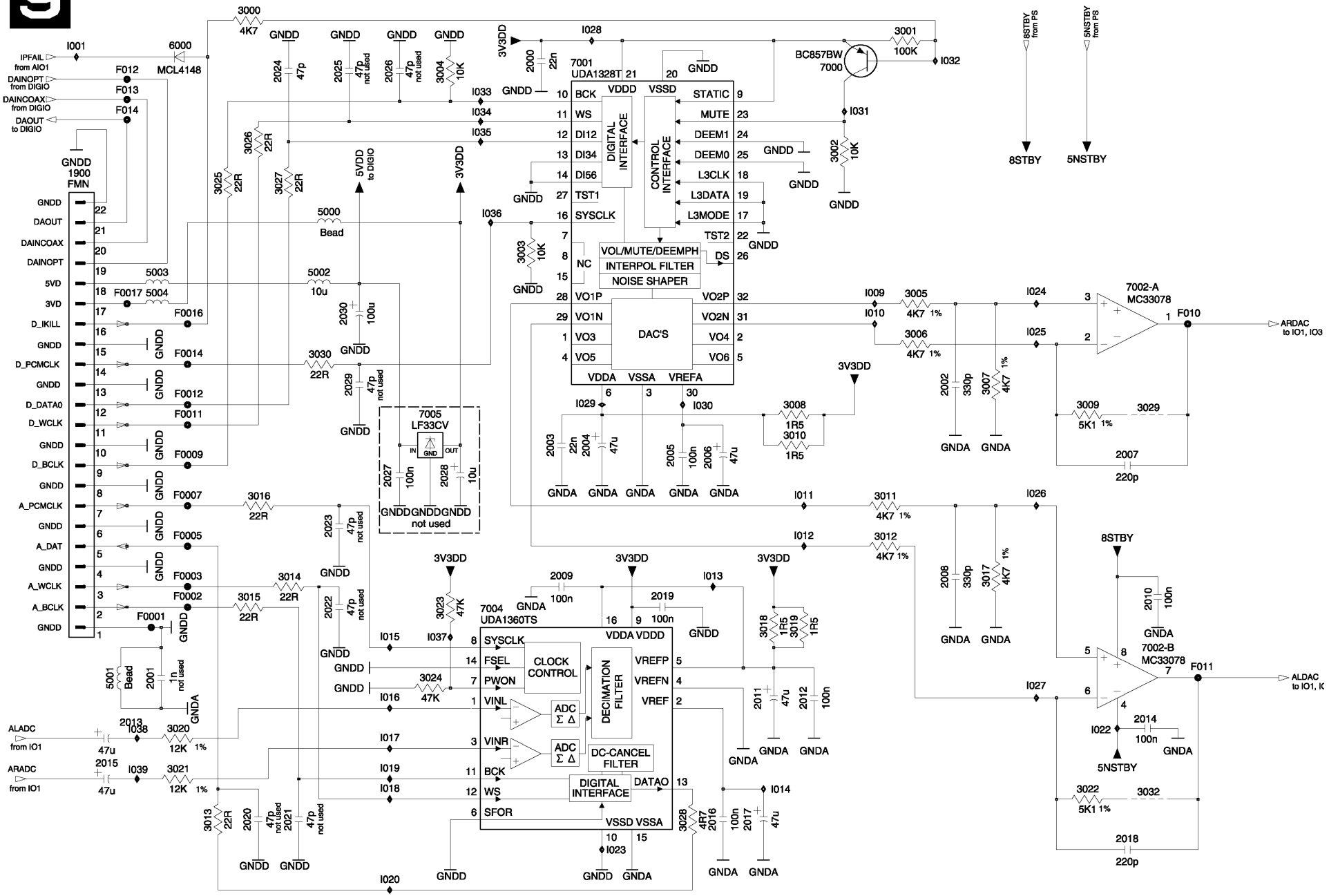

Figure 52 - Audio A/D and D/A Conversion

11 Digital Out

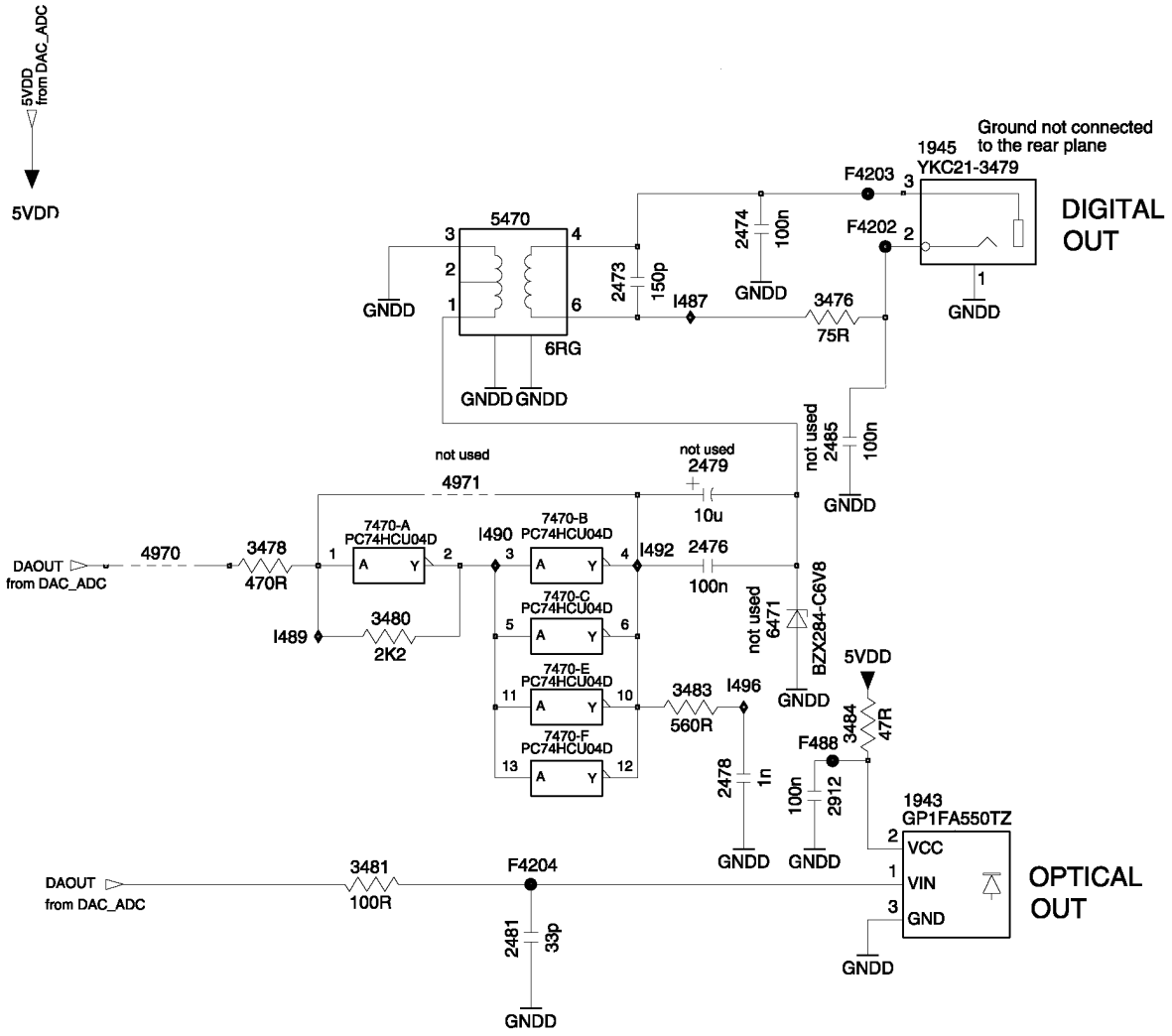

Figure 53 - Digital Input and Output Jacks on the Analog Board

Digital Output

The unit provides two Digital Audio output connections. One uses a coax output connector, and the other uses a fiberoptic connection. The Digital Audio output signal is gated by 7470 and transformer coupled to connector 1945.

The optical output device, receives the same signal as the coaxial output circuit. It is buffererd and is output via, 1943.

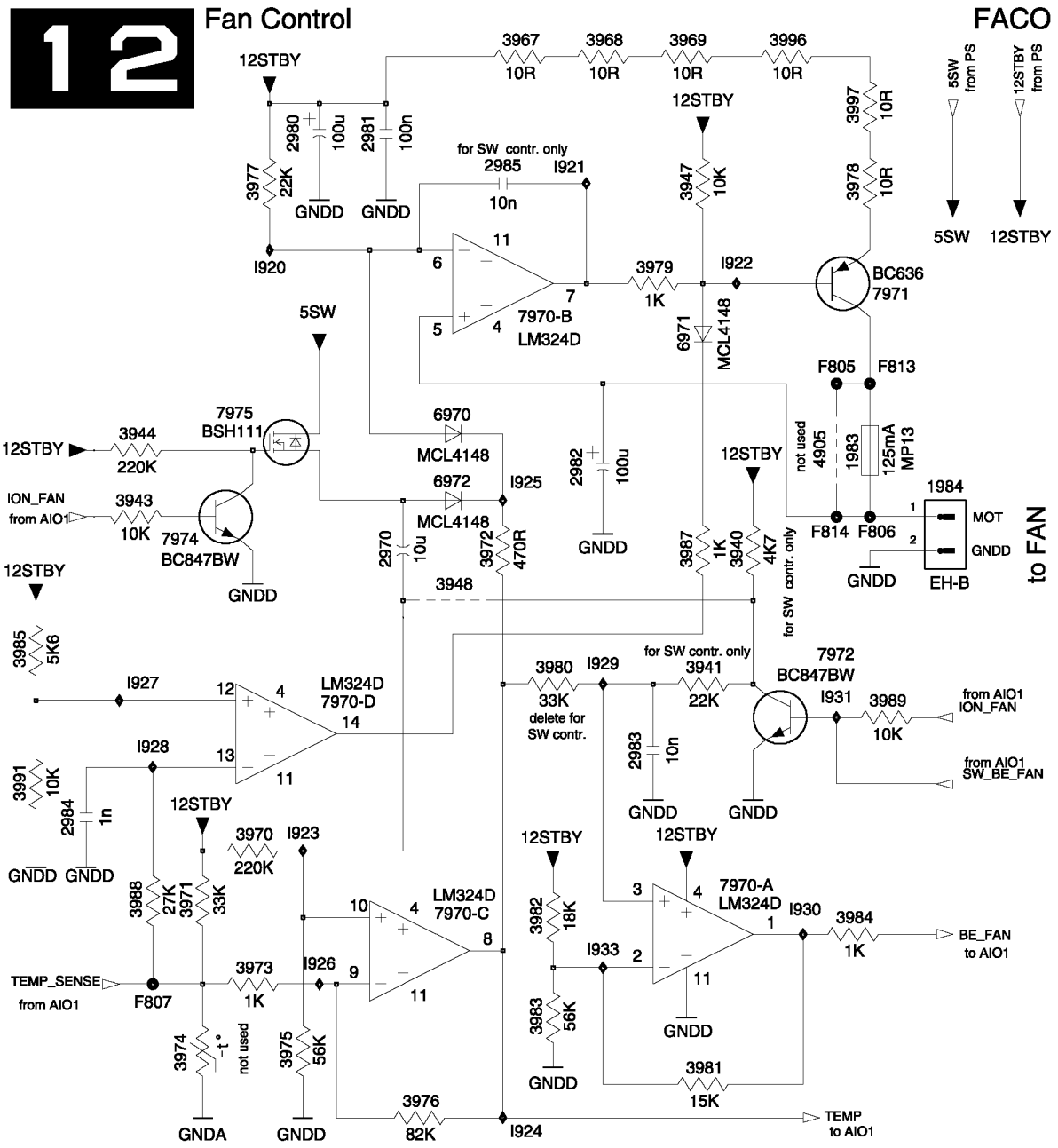

Figure 54 - Fan Control Circuit

Fan Control

The Fan Control circuit is necessary to control the speed of the cabinet fan, 1984, and the BE Fan according to the changes of temperature and motor noise. The temperature is measured via a Negative Temperature Coefficient, NTC, thermistor on the IR Receiver Board, 3135. The sensor's output voltage is labeled Temp_Sense.

The Fan Control circuit uses Op Amps to gain control of the sensor's signal. When the temperature is lower than 25°C the cabinet fan's voltage is approximately. 5V and will reach approximately 10V at a temperature of 40°C. The Microcomputer controls the On/Off function of the two fans via control line ION_FAN and SW_BE_FAN. The TEMP signal goes to the Microcomputer and the inputs of the Op Amps. The Microcomputer supplies the Motor On switching voltages. The speed of both fans are controlled by the Temp_Sense line going into the Op Amps.

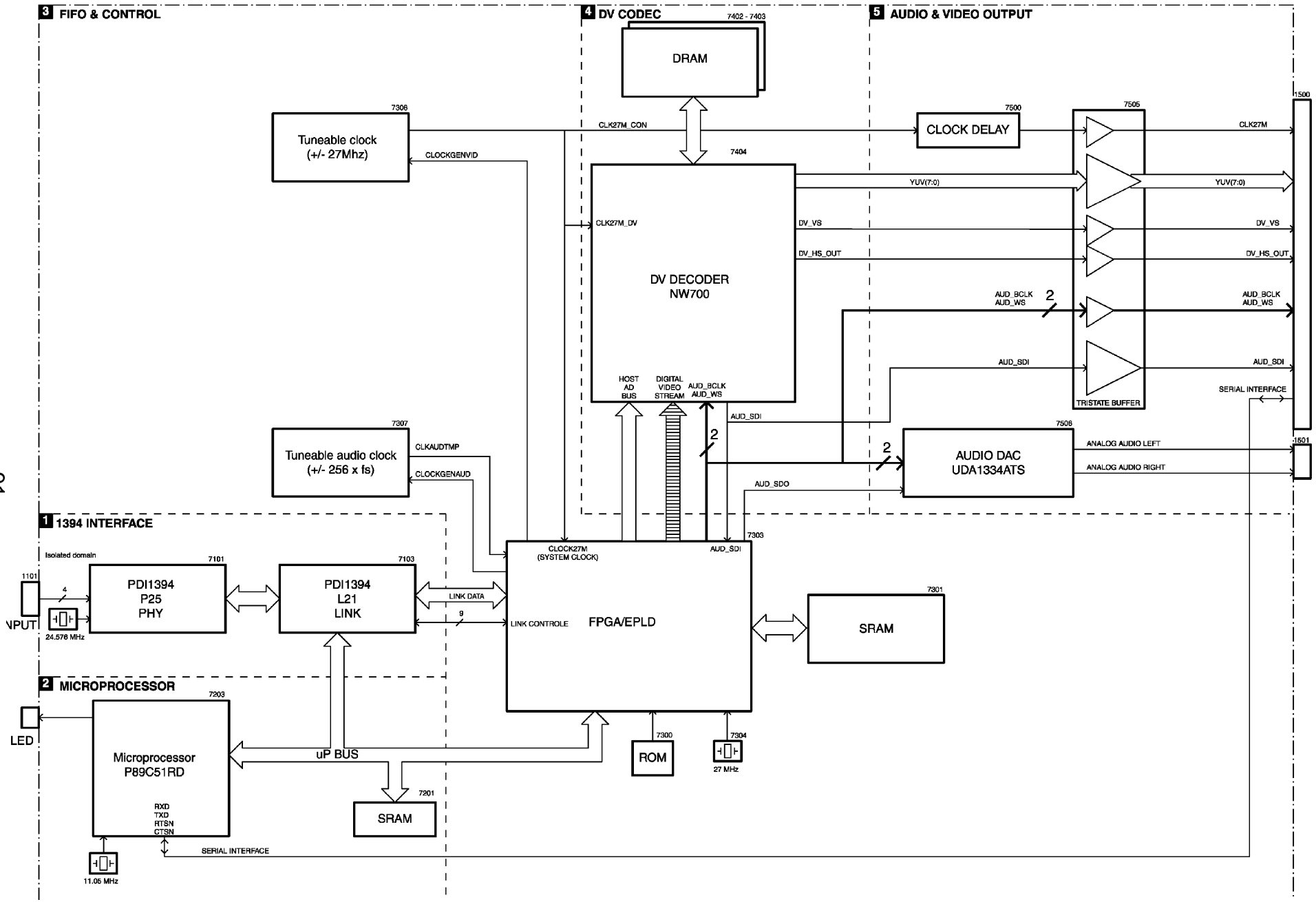

Figure 55 - Digital Input Board Block

Digital Video Input Board

The DVIO Module is a decoder for DV streams. DV from a camcorder, IEEE1394, input stream is converted to CCIR656 Video and Analog Audio (L+R). A serial control interface is present.

Block Diagram

The DVIO module consists of the following blocks, Refer to **Figure 55**. An Independent tunable audio and video clock is used for FIFO and PLL. A Microcomputer using an 8051 CPU with 64 kilobyte of flash memory controls the whole operation. It also has 1 kilobyte of internal data memory. There is a Watchdog timer and PCA outputs. The System Clock runs at 11.0592MHz. On board In Circuit Programming, ISP, can be used to update the EEPROM, Downloading.

Clock Circuit

There are two clocks to consider in the system, the video clock and the audio clock. These two clocks are independent and will be discussed separately. The video clock is approximately 27 MHz. When data is flowing from an external source, it does not have exactly the same frequency and phase. This could cause buffers to under-run or over-run. Since the clock cannot be modified in the source the clock is adjusted to the required frequency and phase to process at the rate of the incoming data. The same requirements apply to the audio clock. The audio clock operates at three frequencies. The source can have a frequency of 8.192 MHz, 11.2896 MHz, or 12.228 MHz. This depends on the sample-rate frequency 32kHz, 44.1kHz, or 48kHz, of the Audio signal.

FIFO and Control

In decode mode, an asynchronous AV-stream is flowing through the IEEE1394 Interface into the FPGA. The FPGA stores the data in a First In First Out buffer. Each buffer holds one whole frame each.

DV Decoder

The AV data goes from the FIFO to the NW700. It decodes the stream into video data in 656 format. The Microcomputer has the ability to read the status registers of the NW700 through the FPGA. By reading these registers extra data from the DV stream, that is not decoded into audio or video, can be sent to the Digital Board, using TXD of the serial interface. This includes Time Stamp and other simular data.

Audio and Video Output

The Audio I^2S data is sent to an Audio DAC, UDA1334. Analog audio Left and Right signals are sent to the Analog Board. The Tri-State Buffer enables the Digital Video stream to go to the Video Input Processor on the Digital Board when the DV source is selected. The clock delay synchronizes the AV clock with the AV data at the output.

1 1394 INTERFACE

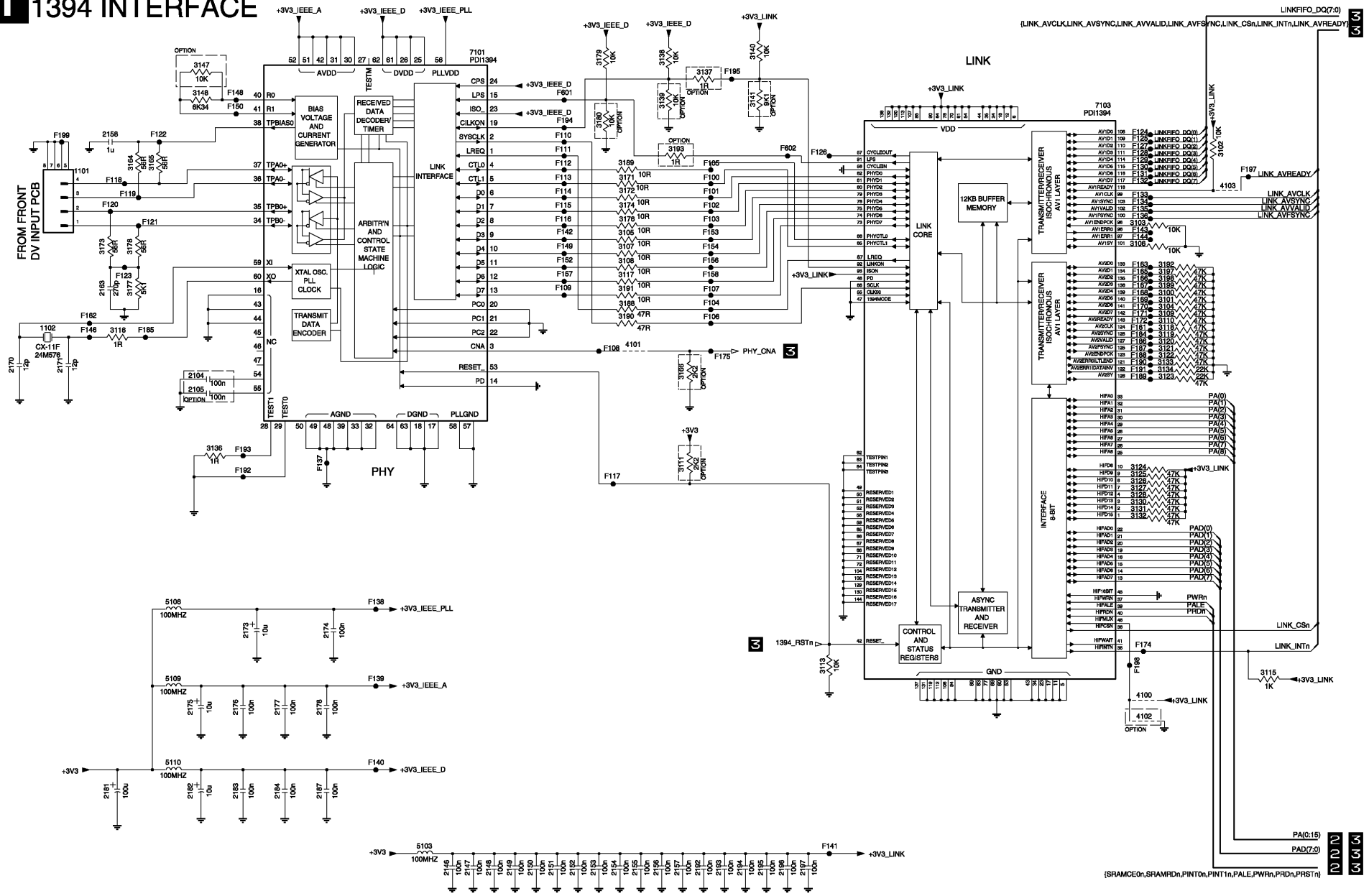

Figure 56 - Asyncronous IEEE Interface

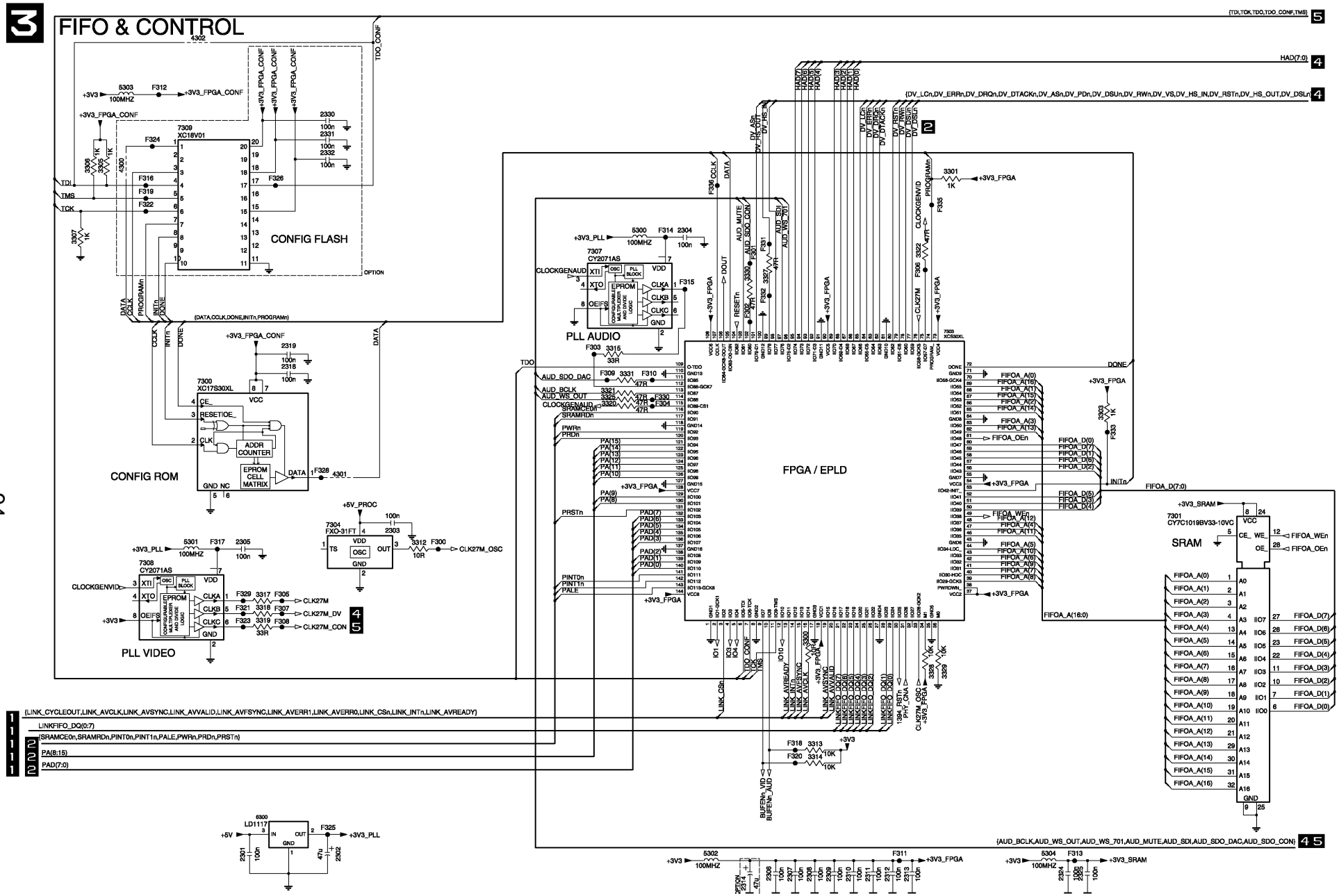

Figure 57 - DIVIO Decoder

4 DVCODEC

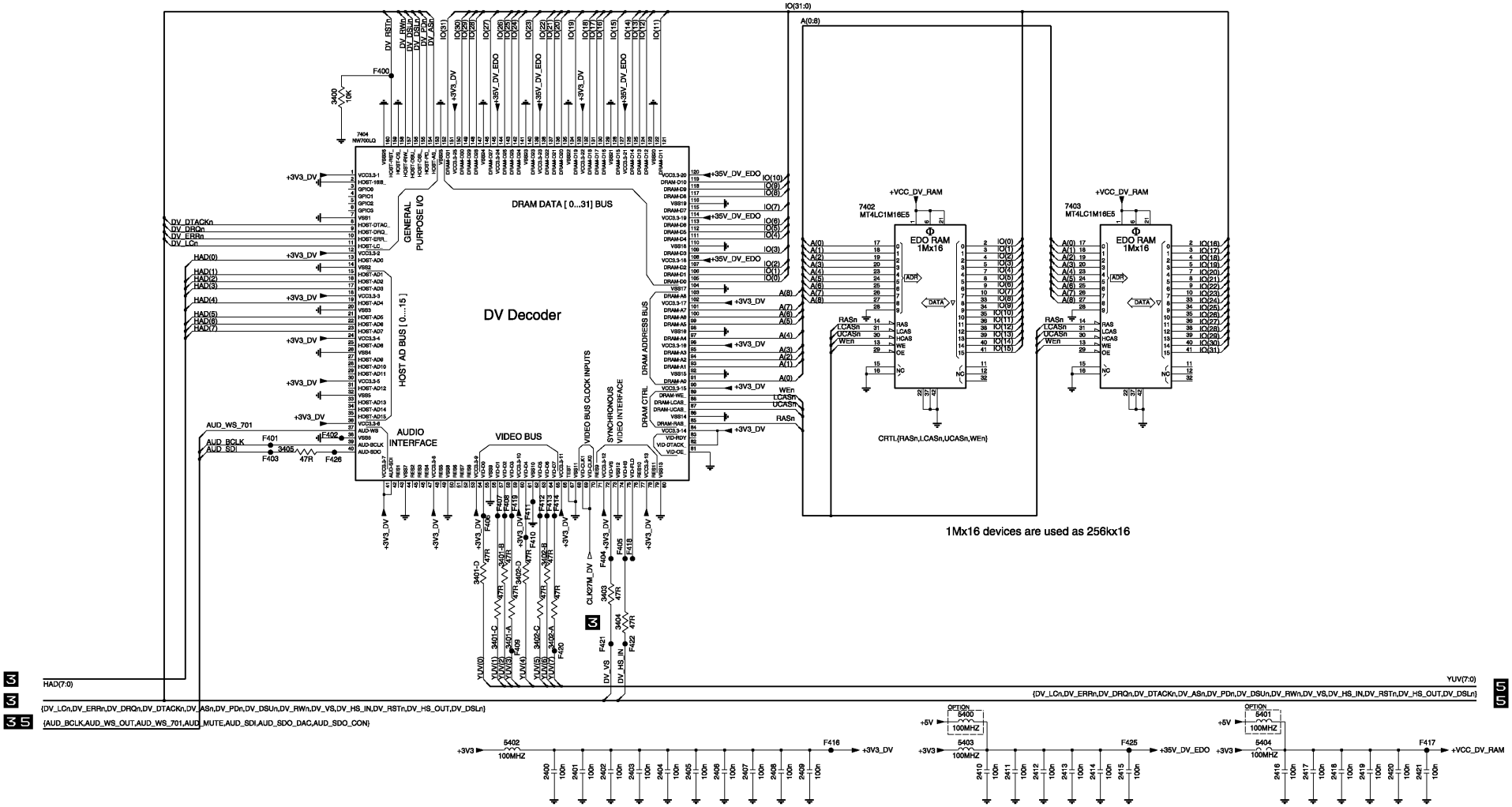

Figure 58 - Digital Video Decoder

5 AUDIO & VIDEO OUTPUT

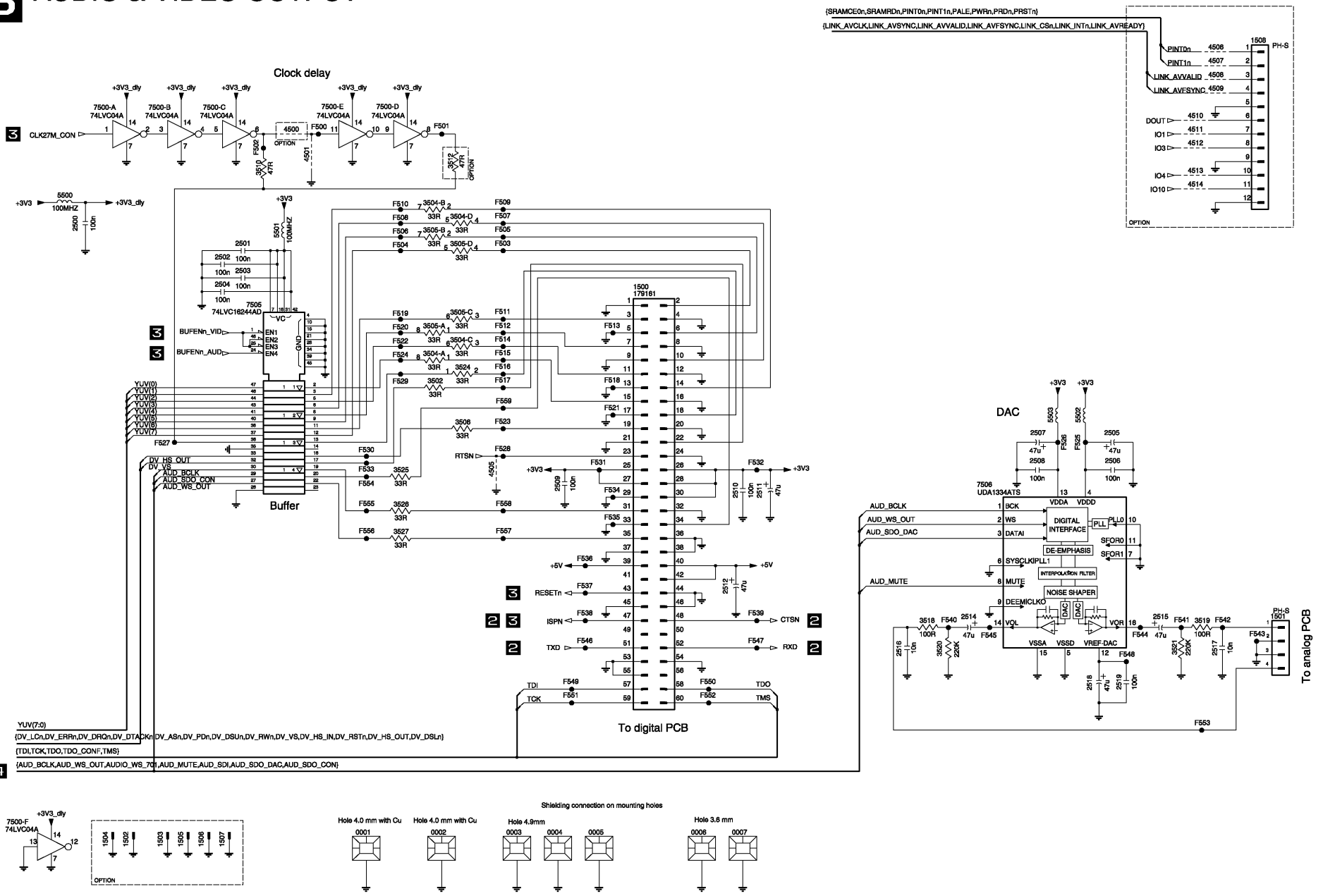

Figure 59 - DIVIO Output

TroubleShooting

The Power Supply

This Power Supply operates whenever AC power is applied. The primary winding of the transformer operates using Hot Ground. Be sure to use an isolation transformer on the AC input supply. When working with Switch Mode Power Supplies, there are three general symptoms to be considered: No operation or dead, improper regulation, and one or more supply lines missing.

No Operation
This symptom can be caused by many components. Of course, check the Standby supplies coming from the SMPS. If you can identify a missing supply, then move on to the next section SPMS problems.

When AC is applied to the unit, The System Control Microcomputer Resets and turns On some of the switched supplies, via the IStndby ON control voltage. The 5VSW and 8VSW supplies are the first group of supplies to be switched On. The Analog Microcomputer Initializes its I^2C bus and communicates with the Tuner, the Audio Demodulator, and the Front Panel. If those circuits operate properly, the ION control voltage goes low to turn on the second set of switched voltages. If the ION switching voltage does not appear, the problem is on the Analog Board or the Front Panel. The Analog Board Microcomputer only allows 10 Seconds for this process. and it will only try once.

If the ION switching voltage appears the Analog Board and the Front Panel are operating well enough to turn on power. The 3.3Vdc is the main supply to most of the microcomputers on many of the PCBs. The Analog Board's Microcomputer also sends out the IReset signal to 7902 on the Digital Board. This IC produces a delayed Resetn signal line for the Host Decoder, the VSM, the VIP, and the Line Doubler. The Host Decoder activates the I^2C Bus on the Digital Board. The Host Decoder also produces four reset signals for: the DIVIO Board, two of them go to the EMPRESS and one to the BE. The Host Decoder expects a response on the I^2C Bus from: the EMPRESS, the VIP, and both Progressive Scan ICs. The BE performs its own reset and self analysis and communicates to the VSM via two signals that it is ready to operate. The SUR line goes Low on Pin 24 of the VSM and the PSEN signal must appear. The PSEN signal is 5.3 MHz. If either the SUR line or the PSEN signal do not appear the, Host Decoder will communicate to the Analog Board's Microcomputer, and the Power will be shut down.

If the BE has responded properly and the rest of the Digital Board operates properly, the Host decoder communicates to the VSM which communicates to System Control Microcomputer on the Analog Board to tell the Front Panel to turn On the Display and wait for customer Keyboard input.

The challenge is to figure out where in this process the machine stops. The Analog Microcomputer allows 10 seconds for the VSM to give the all is well signal. If it does not occur, the ION switching voltage is removed and the unit goes into shutdown.

SMPS Problems
Separate the power Supply from the rest of the unit. Connect it to an isolation transformer. Check for 160Vdc on the drain of 7125. If it is not present, there is an open in the AC input circuit. This includes the bridge rectifier and the primary winding of the transformer.

Next, check the gate of 7125. It should have about 3 - 4 volts on it. If it is near 0Vdc, check two things. Check the FET for a short. And, check the pull up resistors supplying the gate, 3125 and 3126, and 3141. If the voltage is 4Vdc or more, the FET should be conducting.

Check the voltage on the source. It should be a few tenths at most. If it is higher, check the source resistors and the FET. It is a good idea anytime the FET is replaced to replace the source resistors. They can read proper and be out of tolerance, causing a repeat failure in a short time.

Is the unit ticking? Place a scope on the drain of the FET. Is there a signal there? If the signal is about 2 Hz, the Overload Circuit may be activating. Remove AC power and check each of the output lines for a short, and the overload transistors, 7141 and 7143. If no problem can be identified, supply AC and monitor the base of 7143. If it reaches .6V, there is an improper load in the circuit or the FET is shorted.

Improper Regulation

This type fault will show itself in one of three ways: The outputs are too high, the outputs are too low, or alternate high and low outputs. The precise regulation loop monitors the 5Vdc and 3.9Vdc supplies. Measure the voltage drop on the diode portion of the optic coupler, 7200.
If the voltages on the output lines are too high, the voltage drop on the diode portion of the optic coupler should be 1-1.2Vdc. The transistor portion should be conducting hard with little or no voltage drop. If there is a voltage drop on the transistor portion, the optic coupler is bad.

If the transistor portion of the optic coupler has little or no voltage drop, the secondary side of the power supply is asking for less output. The problem involves 7140 and associated components. If 7140 itself checks out, the negative supply to the transistor from 6142 may not be supplying enough control voltage.

If the optic diode has a volt or less, the shunt regulator (7251) and/or the voltage divider resistors can be the problem. Check the diode portion of the optic coupler.

If the voltages on the outputs are too low, the voltage drop on the diode in the optic coupler should be less than a volt. The transistor side should have a 5-6V drop. If these voltages are proper, the secondary portion of the power supply is asking for more output, and the problem is on the primary side.

If the diode portion has a volt or more on it, the Shunt Regulator is improperly driving the optic coupler. The problem is with the Shunt Regulator or the voltage dividers.

If the diode portion does not have a voltage drop of .9V or more and the transistor side has a small voltage drop 3V or less, the transistor portion of the optic coupler is faulty.

For a condition of having alternate high and low output voltages, there is a rectification and filtering problem, or there is an excessive load on one of the output lines. If there is an excessive load on the 5 Vdc line, the 5V could read normal, while the other outputs rise to abnormal levels. The Supply is working harder to maintain the 5V on the monitored line, but the other outputs receive proportionally more energy. This effect makes their output voltage elevated.

For a condition of having just one output missing, there is an open in the Rectification/Filtering circuit. This could include: a fuseable resistor, the winding of the transformer, or problems with the foil pattern on the board. Once the open is identified, measure the line for a short before providing AC to the supply.

The Front Panel/ Display Board

Problems on the Front Panel display fall into four categories: no display function, improper display function, no keyboard function, and no remote control function. Do not consider this board at fault first if all of the symptoms are present. The front panel cannot operate until many functions of self-check pass. A problem on this board more likely shows one of the above symptoms.

The board has several power supply voltages that should be checked first before considering a problem on the board.

No display
There are three major elements to work with for no display: the florescent tube, the Microcontroller and the power supplies dedicated to the tube. The VGNstandy supply is only used by the tube. There is a special switching supply on the Front Panel that supplies filament for the tube.

If the keyboard is operating, the microcomputer is at least partially functioning. Check the dedicated power supply. If it seems normal, check the scanning signals for the tube with a scope. If the supplies are proper and the scanning signals are present, replace the tube. If the scanning signals are not present, the microcomputer becomes suspect.

Improper display
The self diagnostics have a test pattern routine that can help when troubleshooting this type of failure. One of the choices is to light up all of the segments. Set this up to show you what segments are not functioning proper. A pattern should be visible. One row or a column may not be lighting up. Trace out the pin that is responsible for the row or rows that are not lighting. There are diodes connected to these pins. Normally the diode(s) are bad or there is a foreign substance on the board at that location.

No keyboard function
It takes four Microcomputers to function properly for the keyboard to function: the Microcomputer on the Front Panel, the microcomputer on the Analog Board, and two microcomputers on the Digital Board. If the display is working, the Front Panel should be showing four dashes. This means the Power up Reset and self check has passed. Check for remote operation. If the remote functions, start with the Analog Board's microcomputer. Monitor the I^2C Bus while pressing the keyboard. The data should change. If it does, the problem is definitely on the Analog Board. If the I^2C bus does not reflect a change in data when a key is pressed, check the RTL logic for the keys on the Front Panel. If the Keyboard data seems to be getting into the microcomputer, check the secondary switched supplies. The ISTBY goes Low to turn on the SW5 and the SW 8Vdc supplies as part of the last step in power up.

No Remote Control Function
It takes two Microcomputers to function properly for the Remote control to function: the Microcomputer on the Front Panel and the microcomputer on the Analog Board. If the display is working, and keyboard function are normal, the Front Panel Microcomputer and the rest of the unit is operating properly. Start with IR receiver's output. The signal should be TTL level. If it is not, be sure the connections are good, supplying the B+ and ground to the Receiver. If the signal is there, check for it on the Front Panel's Microcomputer, Pin 2. If it is missing check IC7160 and its support components.

If the signal going to the Front panel Microcomputer is proper, monitor the I^2C Bus while pressing the remote keyboard. The data should change. If it does not, check all the vitals to the Microcomputer, VCC, grounds, Clocks, and reset the microcomputer as a test. If none of these yield results, suspect the microcomputer.

The Digital Board

The Digital Board is central to the recorder's operation. There are two categories of symptoms that cause the Digital Board to be suspect. One is "No Power" and the other is a more conventional digital signal flow problem. The reason the Digital Board needs to be focused on for a No Power problem is that the I^2C Bus Host is on the Digital Board. The Host Decoder IC also produces secondary Reset function for many ICs including the BE. If you are concerned with "No Power" and the SMPS is functioning, go to the No power part of this write up where all the circuits involved in power up will be discussed. For digital signal path troubleshooting, proceed to the next paragraph.

Close scrutiny of the symptom is necessary. If you are considering the problem to be on the Digital board, you have basic operation of the unit. The unit powers up. The Front Panel's display is proper. The unit will try to play a disc. The symptom involves: no menu, no playback Video or Audio, no record Video or Audio, or scrambled Video or Audio. If you can play a known good disc, you can eliminate half of the circuitry in the Digital Signal Processor. If you see the Video and Audio during the record process, the Digital Board is probably not where your problem is. The parallel loop thru condition that occurs during record utilizes most of the circuitry on the Digital Board and the Analog Board.

If the problem is apparent in playback, use playback for troubleshooting. Use a disc that has colorbars recoded on it. Check the CVBS signal on the output of the Host Decoder. The Bars signal allows you to closely scrutinize the signal on the output. If the signal is good, follow the signal through the Analog Board to the output jacks.
If the signal is missing or distorted, check the DC voltage on the Output Pin. If the DC voltage is .5V or less, the signal could be loaded down. Open the connection to the audio board to separate where the problem is.

If the unit plays back properly, use the record mode to troubleshoot. Most of the playback circuitry is in operation as well. The output of the VSM supplying the BE is in the middle of the circuitry on the Digital Board. Check the Digital Video stream here. If it is not present, check for it going to the Empress. If it is there, the problem involves the Empress and/or the VSM. If the signal is not present on the inputs to the Empress, check the inputs to the VIP. If the signals are there, stay on the Digital Board, checking for problems with the VIP and/or the Empress. If the signals are not coming into the VIP, the problem is on the Analog Board. For all of these checks you are looking for clean digital transitions of the signal.

The Analog Board

The Analog Board can display many symptoms. There are three main categories to consider when looking for a problem on the Analog Board: no Power, one or more function inoperative, or a Video/Audio switching problem. If you are working with a No Power problem, go to the No Power portion of this write up. If you are working with a single function that is not operative, trace the control of the function to the System Control IC. For a Video/Audio routing issue, continue with the next paragraph.

It has many inputs and outputs. It contains the Tuner function. Symptoms for this module will be: one or more type of output is missing, or the Tuner does not function properly. Each of the inputs and outputs have separate paths in and out of the module. They all, however, pass through the massive switch, IC7507. The key to an input/output problem will be determining which inputs and outputs are affected. If it is a single signal, follow that line through the circuitry to determine where the signal stops. If more than one signal or all the signals are not passing through the board, 7507 is the place to start.

Tuner problems
This symptom involves two major components, the Tuner and the Demodulator IC7703. Tuner problems fall into two categories: no Tuner function or erratic Tuner function. Be-aware: the RF block on the unit does not contain an RF modu-

lator. The RF signal merely loops through. Tuner operation needs to be checked on the Video Outputs.

No Tuner Functions
As with any circuit, verify the supply voltages. The 33Vdc supply is used exclusively by the Tuner. Check for the presence of the I^2C Buss on the Tuner. This signal controls the operation of the Tuner. If those two conditions are met, there should be IF going to the demodulator IC. If possible provide a substitute IF signal to check the Demodulator IC. If substitution shows the Demodulator is good, replace the Tuner. If no substitution is available, Noise can be introduced into the IF signal path. The demodulator should show a change in the output.

Erratic Tuner Function
Problems described here usually are: the Tuner drifts or won't lock in, certain bands of the Tuner do not function. or, the picture is snowy. Slow lock in or continuous hunting for lock in is usually the SAW filter, 1701. In rare cases, the AFC Adjustment will cure it. If both of those have been tried, check or replace the components on Pins 6,7,18, and 19. If no results are achieved, replace the Demodulator IC before the Tuner.

When it is proven that the Demodulator IC or circuits to follow are the problem, check for Video on Pin 16 for Video. This assures us that the problem is here and not further down the signal chain. Most of the components around the demodulator IC are passive. The IC is the main suspect. You should prove the IC is bad before replacing. Using an ohmmeter, check every pin of the IC to ground, looking for a short or near short. If nothing is found, it is reasonable to consider the IC bad.

Basic Engine

If the PSEN signal is not present, there is a problem in the BE that will interfere with the unit powering up. Other symptom caused by the BE can be playability and Recording Problems.

No power up involves the MACE3 Microcomputer. It is the System Control for the BE. Like any microcomputer, first check the supplies, the Oscillator, and the Reset to the IC. Then check for the SUR line. It Goes low after the MACE3 checks its memory. If it doesn't go low, the MACE3, the SRAM, or the Flash Rom are bad. If the MACE oscillator is present, at least part of the Chip is functioning. Check for data on the Flash ROM. It is read first. If there is activity, suspect the SRAM. If there is no activity on the FLASH suspect the Flash ROM as bad.

If the Symptom has in the display three words repeating" Opening, Closing, Blocked", the problem is likely the OPU. Those three words could appear when a tray motor problem is occurring, however, the OPU is a much more common occurrance.

There are many symptoms that involve playability, and recordability. Most common is that the unit will not recognize a disk, or a certain type of disk. Sometimes the symptom is that the unit writes or reads for only a few minutes then an error is shown in the display. Another is that the unit has a problem during the Menu update. All of these symptoms and more are usually caused by a bad OPU.

Edit Problems and Chapter problems have two issues to be resolved. One is the software. There have been many updates to the System software. Many of the updates were designed to fix those kind of issues. FF12p is the current version to be loaded. If the Software upgrades does not fix the problem, It is likely the OPU is the problem.

List of Abbreviations

+12V	+12V Power Supply
+2V5_FLI	+2V5 Power Supply for FLI
+2V5_PLL	+2V5 Power Supply for PLL
+3V3	+3V3 Power Supply
+3V3_ANA	+3V3 Power Supply Analog
+3V3_DD	+3V3 Power Supply Digital
+3V3_DLY	+3V3 Power Supply for IC7500
+3V3_DV	+3V3 Power Supply for IC7404
+3V3_FLI	+3V3 Power Supply for FLI
+3V3_FPGA	+3V3 Internal Power Supply for IC7303
+3V3_FPGA_CONF	+3V3 Power Supply for IC 7300
+3V3_IEEE_A	+3V3 Digital Power Supply for PHY IC 7101
+3V3_IEEE_PLL	+3V3 PLL Power Supply for PHY IC 7101
+3V3_LINK	+3V3 Power Supply IC7103
+3V3_PLL	+3V3 Power Supply IC7307 & IC7308
+3V3_SRAM	+3V3 Power Supply
+5V	+5V Power Supply
+5V_BUFFER	+5V Power Supply for Video Filters
+5V_PROC	+5V Power Supply IC7200, IC7201, IC7203 & IC7208
+VCC_DV_RAM	+3V3 Power Supply for DV_RAM (IC7400—> IC7404)
1394_RSTN	Reset of LINK IC (7103) and PHY IC (7101)
5508_HS	Horizontal Synchronization from Host Decoder to Progressive Scan
5508_ODD_EVEN	Odd - Even control from Host Decoder to Progressive Scan
-5V	-5V Power Supply
-5V_BUFFER	-5V Power Supply for Video Filters
+35V_DV_EDO	+3V3 Power Supply EDO Bus IC7404 A (0:8) Address lines
A1, A2	Power Calibration maximum and Minimum signals
A_EMPRESS (13:0)	EMPRESS Address Output to SDRAM
ACC_ACLK_OSC	Audio Clock PLL Output Sync with incoming Video for record
ACC_ACLK_PLL	Audio Clock PLL Output for play back
ACLK_EMP	EMPRESS Audio Clock Output
AD_ACLK	Audio Decoder Clock
AD_BCLK	Audio Decoder I^2S bit Clock
AD_DATAO	Audio Decoder Output Data (PCM)
AD_SPDIF33	Audio Digital Output to the Analog Board
AD_WCLK	Audio Decoder I^2S word Clock
ADIP	Address in Pregroove
ADC	Analog to Digital Conversion
AE_ACLK	Audio Encoder Clock
AE_ACLK_OEN	Audio Encoder Clock Output Enable
AE_BCLK	Audio Encoder I^2S bit Clock
AE_BCLK_DV	Audio Encoder I^2S bit Clock to DVIO
AE_BCLK_VSM	Audio Encoder I^2S bit Clock to VSM
AE_DATAI	Audio Encoder Input Data (PCM)
AE_DATAI_DV	Audio Encoder Input Data (PCM) from DVIO

AE_DATAO	Audio Encoder Output Data (PCM)
AE_WCLK	Audio Encoder I^2S word Clock
AE_WCLK_DV	Audio Encoder I^2S word Clock to DVIO
AE_WCLK_VSM	Audio Encoder I^2S word Clock to VSM
ANA_WE	Analog write Enable Decoder
ANA_WE_LV	Analog write Enable Low Voltage
AUD_BCLK	Audio Bit Clock
AUD_MUTE	Audio Mute
AUD_SDI	Audio Serial Data Input
AUD_SDO_CON	Audio Serial Data Output to buffer IC 7505
AUD_SDO_DAC	Audio Serial Data Output to DAC IC 7506
AUD_WS_701	Audio Word Select to DV CODEC IC 7404
AUD_WS_OUT	Audio Word Select to buffer IC 7505
AWSOME	Adip decoding Wobble processing Error correction Synchronous start/stop and Occasionally Mend Errors
B_IN_VIP	Video blue Input to Video Input Processor
B_OUT	Video blue Output from Host
B_OUT_B	Filtered blue Video Output
BA	Bank Address
BCLK_CTL_SERVICE	Bitclock control Service Interface
BE_BCLK	Basic Engine I^2S bit Clock
BE_BCLK_VSM	Basic Engine I^2S bit Clock to VSM
BE_CPR	Basic Engine Control Processor ready to accept Data
BE_DATA_RD	Basic Engine Data read
BE_DATA_WR	Basic Engine Data write
BE_FAN	Basic Engine FAN
BE_FLAG	Basic Engine error flag
BE_IRQN	Basic Engine interrupt request
BE_LOADN	Basic Engine LOAD (LOW active)
BE_RXD	Basic Engine S2B received Data
BE_SUR	Basic Engine Servo Unit Ready to accept Data (S2B)
BE_SYNC	Basic Engine sector/abs time Sync
BE_TXD	Basic Engine S2B transmitted Data
BE_V4	Basic Engine versatile Input pin
BE_WCLK	Basic Engine I^2S word Clock
BE	Basic Engine/Mechanism-Servo Board
BUFENN_AUD	Buffer Enable Audio
BUFENN_VID	Buffer Enable Video
C_IN	Video Chrominance Input
C_IN_VIP	Chrominance Input to Video Input Processor
C_OUT	Chrominance Output from Host Decoder
C_OUT_B	Filtered Chrominance Output
CALF	Laser Calibration Final voltage
CAS	Column Address strobe
CAV	Constant Angular Velocity
CB_OUT (9:0)	Chrominance Blue out
CCLK	Configuration Clock
CLK4	SDRAM Clock

CLK27M	27MHz Clock
CLK27M_CON	27MHz Clock to Digital Board
CLK27M_DV	27MHz Clock Digital Video Codec
CLK27M_OSC\	27MHz Clock IC7304
CLOCKGENAUD	Clock generator Audio
CLOCKGENVID	Clock generator Video
CLV	Constant Linear Velocity
ComPair	Computer aided rePair
Cosphi	Cosine Position of Hall info
CPUINT0	Control processor unit interrupt
CPUINT1	Control processor unit interrupt
CPR	Control Processor Ready
CR_OUT (9:0)	Chrominance Red out
CS	Chip Select
CTS1P	Clear to send (Service Interface)
CTSN	Clear to Send
CVBR	CD Variable Bit Rate recording
CVBS_OUT	Composite Video Output out of the Host Decoder
CVBS_OUT_B	Filtered Composite Video Output
CVBS_OUT_B_VIP	Composite Video to Video Input Processor (Digital Board Video loop)
CVBS_Y_IN	Composite Video/Luminance Input
CVBS_Y_IN_A	Composite Video/Luminance Input to Video Input Processor
CVBS_Y_IN_B	Composite Video/Luminance Input to Video Input Processor
CVBS_Y_IN_C	Composite Video/Luminance Input to Video Input Processor
D_ADDR (10:0)	Address bus
D_DATA (29:0)	Data bus
D_EMPRESS (15:0)	SDRAM Data Input/Output of EMPRESS
D_PAR_D (7:0)	Front-end parallel interface Data (record)
D_PAR_DVALID	Front-end parallel interface Data valid
D_PAR_REQ	Front-end parallel interface request
D_PAR_STR	Front-end parallel interface strobe
D_PAR_SYNC	Front-end parallel interface Sync
DAC	Digital to Analog Converter
DAIO	Digital Audio Input/Output
DATA	Data from config ROM
DENC	Digital Encoder
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DONE	Indication of the completion of the configuration process
DOUT	Serial configuration Data Output
DRAM	Dynamic RAM
DROPPI	DVD Rewriteable OPU Pre-Processor IC
DSD	Direct Stream Digital
DSP	Digital Signal Processor
DV_ASN	DVCODEC Address Strobe
DV_DRQN	DVCODEC Data Request Interrupt
DV_DSLN	DVCODEC Data Strobe Lower 8 bits
DV_DSUN	DVCODEC Data Strobe Upper 8 Bits
DV_DTACKNDVCODEC	Data Transfer Acknowledge
DV_ERRN	DVCODEC Error Interrupt

DV_HS_IN	DVCODEC Horizontal synchronization In
DV_HS_OUT	DVCODEC Horizontal synchronization Out
DV_IN_CLK	Digital Video in Clock from DVIO Board
DV_IN_DATA (7:0)	Digital Video in Data bus from DVIO Board
DV_IN_HS	Digital Video in horizontal synchronization from DVIO Board
DV_IN_VS	Digital Video in vertical synchronization from DVIO Board
DV_LCN	DVCODEC Last Code Interrupt
DV_PDN	DVCODEC Power Down
DV_RSTN	DVCODEC System Reset for NW701
DV_RWN	DVCODEC Read/Write control signal
DV_VS	DVCODEC Vertical synchronization
EFM	Eight to Fourteen bit Modulation
EMI_A (21:1)	External Memory Interface Address Bus (Host Decoder)
EMI_BE0N	External Memory Interface Lower byte Enable (Host Decoder)
EMI_BE1N	External Memory Interface Upper byte Enable (Host Decoder)
EMI_CAS0N	External Memory Interface SDRAM column Address strobe
EMI_CE1N	External Memory Interface VSM Lower bank Enable
EMI_CE2N	External Memory Interface VSM Higher bank Enable
EMI_CE3N	External Memory Interface flash IC's Enable
EMI_D (15:0)	External Memory Interface Data Bus (Host Decoder)
EMI_PROCCLK	External Memory Interface Processor Clock (Host Decoder)
EMI_RWN	External Memory Interface Read/Write control signal (Host Decoder)EMI_WAIT
	External Memory Interface Wait state request (Host Decoder)
EMPRESS_BOOT	EMPRESS BOOT select Input
EMPRESS_IRQN	EMPRESS Interrupt request Output
FDS	Full Diagnostic Software
FIFO	First In First Out memory
FIFOA_A (0:15)	FIFO buffer A Address bus
FIFOA_OEN	FIFO buffer A Output Enable
FIFOA_WEN	FIFO buffer A Write Enable
FLASH_OEN	FLASH Output Enable control signal
FPGA	Field Programmable Gate Array
FTC	Fast Track Count
G_IN_VIP	Video green Input to Video Input Processor
G_OUT	Video green Output from Host Decoder
G_OUT_B	Filtered green Video Output from Host Decoder
GNDD	Digital Ground
HD_M_AD (13:0)	Host Decoder SDRAM Address bus
HD_M_CASN	Host Decoder SDRAM column Address strobe
HD_M_CLK	Host Decoder SDRAM Clock
HD_M_CS0N	Host Decoder SDRAM chip select
HD_M_DQ (15:0)	Host Decoder SDRAM Data bus
HD_M_DQML	Host Decoder SDRAM Data mask Enable (Lower)
HD_M_DQMU	Host Decoder SDRAM Data mask Enable (Upper)
HD_M_RASN	Host Decoder SDRAM row Address strobe
HD_M_WEN	Host Decoder SDRAM write Enable
HF	High Frequency/signal from the disc
HSOUT	Horizontal synchronization OUT
I^2C	I^2C/serial communication protocol

I^2S	Integrated IC Sound Buss (3.3V High)
INITN	Initiate Configuration
IO (0:30)	Data bus of IC7404
ION	Inverted ON: Enable the power Supply for the Digital Board when LOW
IRESET_DIG	Initialization of the Digital Board, HIGH when power ON
ISPN	In System Program Line (used for programming IC7203)
JTAG3_TCK	JTAG Test Clock
JTAG3_TD_VIP_TO_VE	JTAG Transmitted Data Video Input Processor to Video Encoder
JTAG3_TD_VSM_TO_VIP	JTAG Transmitted Data Versatile Stream Manager to Video Input Processor
JTAG3_TMS	JTAG Test Mode Select
JTAG3_TRSTN	JTAG Test part ResetN
LADIC	LAser Drive IC
LCASN	Lower Column Address strobe for IC7404 DRAMS
LDON	Laser Drive On
LINK_AVCLKLINK IC	Audio/Video Interface Clock
LINK_AVFSYNC	LINK IC Audio/Video frame Sync
LINK_AVREADY	LINK IC Audio/Video Data ready to send
LINK_AVSYNC	LINK IC Audio/Video packet Sync
LINK_AVVALID	LINK IC Audio/Video Data valid
LINK_CSN	LINK IC chip select
LINK_INTN	LINK IC interrupt
LINKFIFO_DQ (0:7)	Audio Video Data interface
LLD	Loss Less Decoder
LLP	Laser Low Power
LOAD_DVN	LOAD Digital Video (LOW active)
LPCM	Linear Pulse Code Modulation
LRCLK	Left/Right Clock
MACE	Mini All CD Engine
Mpeg	Motion Picture Experts Group (compression scheme)
MUTEN	Mute Enable
MUTEN_LV	Mute Enable Low Voltage
NVM	Non Volatile Memory
OPC	Optimum Power Cailibration
ORD	Radial Drive disable
OPU	Optical Pickup Unit
P_SCAN_YUV (7:0)	Progressive Scan Digital Video bus
PA (0:15)	SRAM processor Address
PCS	Position Control Sled
PCM	Pulse Code Modulation
PPN	Wobble Pre-Processor signal
PPNO	Wobble Pre-Processor signal Output signal
PWRN	Processor write
SYSCLK_VSM_5508	System Clock VSM and Host decoder
PAD (0:7)	SRAM processor Data
PALE	Processor Address Latch Enable
PHY_CAN	PHY 1394 cable not active
PHY_LPS	LINK IC power status
PINT0N	Processor interrupt 0

PINT1N	Processor interrupt 1
PRDN	Processor read
PROGRAMN	Low active Input to initiate a configuration cycle
PRSTN	Processor reset
R_IN_VIP	Video Red Input to Video Input Processor
R_OUT	Video Red Output from Host Decoder
R_OUT_B	Filtered Red Video Output from Host Decoder
RAS	Row Address Strobe
RASN	Row Address strobe Enable
Refsin	Reference voltage for Hall sensor amp
Refcos	Reference voltage for Hall sensor amp
RESETN	Reset Host Decoder
RESETN_BE	System reset basic engine (buffered)
RESETN_DVIO	System reset Digital Video Input Output (buffered)
RESETN_VE	System reset Video Encoder
ROMH_CEN	Flash 2 chip Enable
ROML_CEN	Flash 1 chip Enable
RSTN_BE	Reset control of basic engine
RSTN_DVIO	Reset control of DVIO
RSTAT	Status Read
RTS1P	Ready To Send Data to service serial interface
RTSN	System Reset
RXD	Receive Data
RX1P	Receive Data from service serial interface
S2B	Serial to Basic Engine Communication
SCL	I^2C bus Clock
SD_CASN	SDRAM Column Address strobe Output (active LOW)
SD_CLK	SDRAM Clock Output
SD_CLKE	SDRAM Clock Enable Output
SD_CSN	SDRAM
SD_DQM (1:0)	SDRAM Data mask Enable Output
SD_RASN	SDRAM row Address strobe Output
SD_WEN	SDRAM write Enable Output
SDA	I^2C bus Data
SEL_ACLK1	Select Audio Clock (playback)
SDRAM	Synchronous DRAM
Sinphi	Sine Position of Hall info
SM_CS3N	SRAM chip select
SM_LBN	SRAM lower bank strobe
SM_OEN	SRAM Output Enable
SM_UBN	SRAM upper bank
SM_WEN	SRAM write Enable
SMA (17:0)	SRAM Address Output
SMD (15:0)	SRAM Data Input/Output
SPDIF	Sony Philips Digital Interface for Audio
SPIDRE	Signal Processing IC for DVD REwritable
SRAM	Static Random Access Memory
SRAMCE0N	SRAM processor chip Enable 0
SRAMRDN	SRAM processor Output Enable

SVCD	Super Video CD
Subcode	Tacking information/Track number/and disc location information
SYSCLK_EMPRESS	System Clock EMPRESS
SYSCLK_PROGSCAN	System Clock Progressive Scan
TCK	Boundary scan Test Clock
TDI	Boundary scan Test Data Input
TDO	Boundary scan Test Data Output
TDO_CONF	Boundary scan Test Data Output from IC 7309
TLL	Track Loss signal
TMS	Boundary scan Test Mode Select
TPI	Track Position Indicator
TX1P	Transmit Data to service serial interface
TXD	Transmitted Data
U_IN	Video U Input
U_IN_VIP	Video U Input to Video Input Processor
UCASN	Upper column Address
V_IN	Video V Input
V_IN_VIP	Video V Input to Video Input Processor
VBR	Variable Bit Rate recording
VCC3_CLK_BUF	Power Supply 3V3 Clock buffer
VCC3_VSM	Power Supply 3V3 Versatile Stream Manager
VCC3_VSM_MEM	Power Supply 3V3 Versatile Stream Manager Memory
VCC5_4046	Power Supply 5V to PLL IC
VDD_125	Power Supply 5V to buffer 7202
VDD_CORE	Sti5508 Core Supply voltage 2.5V
VDD_EMP	Empress Supply voltage 3.3V
VDD_EMP_CORE	Empress Core Supply voltage 2.5V
VDD_FLASH_H	Flash 7301 Supply voltage
VDD_FLASH_L	Flash 7302 Supply voltage
VDD_LVC32	Power Supply LVC32
VDD_PCM	Power Supply Audio decoder of Sti5508
VDD_PLL	Power Supply PLL Audio decoder of Sti5508
VDD_RGB	Power Supply Video encoder of Sti5508
VDD_STI	Power Supply of Sti5508
VDD_YCC	Power Supply Video encoder of Sti5508
VDD5_MK2703	Power Supply MK2703
VDD5_OSC	Power Supply Oscillator
VDDA1A_7118	Power Supply for Analog Input of VIP
VDDA2A_7118	Power Supply for Analog Input of VIP
VDDA3A_7118	Power Supply for Analog Input of VIP
VDDA4A_7118	Power Supply for Analog Input of VIP
VDDE_7118	Power Supply Digital for peripheral cells of VIP
VDDI_7118	Power Supply Digital for core of VIP
VDDX_7118	Power Supply for crystal oscillator of VIP
VE_DATA (7:0)	Video Encoder Data Bus
VE_DSN	Video Encoder Data Strobe
VE_DTACKN	Video Encoder Data Transfer acknowledge
VIP_ERROR	Video Input Processor error
VIP_FB	Video Input Processor Fast Blanking
VIP_FID_FF	Video Input Processor field identifier to Flip Flop

VIP_HS	Video Input Processor horizontal synchronization
VIP_ICLK	Video Input Processor Input Clock
VIP_IDQ	Video Input Processor Output Data qualifier
VIP_IGP1	Video Input Processor Input general purpose 1
VIP_INT	Video Input Processor interrupt
VIP_RTS1	Video Input Processor ready to send
VIP_VS	Video Input Processor vertical synchronization
VIP_YUV (7:0)	Video Input Processor Digital Video (CCIR 656)
VS_IN	Vertical synchronization IN
VSM_M_A (13:0)	Versatile Stream Manager SDRAM Address bus
VSM_M_CASN	Versatile Stream Manager SDRAM column Address strobe
VSM_M_CLKEN	Versatile Stream Manager SDRAM Clock Enable
VSM_M_CLKOUT	Versatile Stream Manager SDRAM Clock out
VSM_M_D (15:0)	Versatile Stream Manager SDRAM Data bus
VSM_M_LDQM	Versatile Stream Manager SDRAM lower Data mask Enable
VSM_M_RASN	Versatile Stream Manager SDRAM row Address strobe
VSM_M_UDQM	Versatile Stream Manager SDRAM upper Data mask Enable
VSM_M_WEN	Versatile Stream Manager SDRAM write Enable
VSM_UART1_CTSN	Versatile Stream Manager UART1 clear to send to Analog Board (UART1 is gateway to Analog Board)
VSM_UART1_RTSN	Versatile Stream Manager UART2 clear to send to DVIO Board (UART2 is gateway to DIVIO Board)
VSM_UART1_RX	Versatile Stream Manager UART1 ready to send to Analog Board
VSM_UART1_TX	Versatile Stream Manager
VSM_UART2_CTSN	Versatile Stream Manager UART1 received Data to Analog Board
VSM_UART2_RTSN	Versatile Stream Manager UART2 received Data to DVIO Board
VSM_UART2_RX	Versatile Stream Manager UART1 transmitted Data to Analog Board
VSM_UART2_TX	Versatile Stream Manager UART2 transmitted Data to DVIO Board
VSOUT	Vertical synchronization OUT
WE	Write Enable
WEN	Write Enable control signal to SRAM
Wobble	The spiral track stamped into recordable discs
Y_IN	Luminance Input from Analog Board
Y_OUT	Luminance Output from Host Decoder
Y_OUT_B	Filtered luminance Output
YY_OUT (9:0)	Luminance Output from FLI

Written by Dan Crum
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